Block I
Apollo Guidance Computer (AGC)

How to build one in your basement

Part 5: Input/Output (IO) Module

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December, 2004

Abstract

This report describes my successful project to build a working reproduction of the 1964 prototype for the Block I Apollo Guidance Computer. The AGC is the flight computer for the Apollo moon landings, and is the world's first integrated circuit computer.

I built it in my basement. It took me 4 years.

If you like, you can build one too. It will take you less time, and yours will be better than mine.

I documented my project in 9 separate .pdf files:

Part 1 Overview: Introduces the project.

Part 2 CTL Module: Design and construction of the control module.

Part 3 PROC Module: Design and construction of the processing (CPU) module.

Part 4 MEM Module: Design and construction of the memory module.

Part 5 IO Module: Design and construction of the display/keyboard (DSKY) module.

Part 6 Assembler: A cross-assembler for AGC software development.

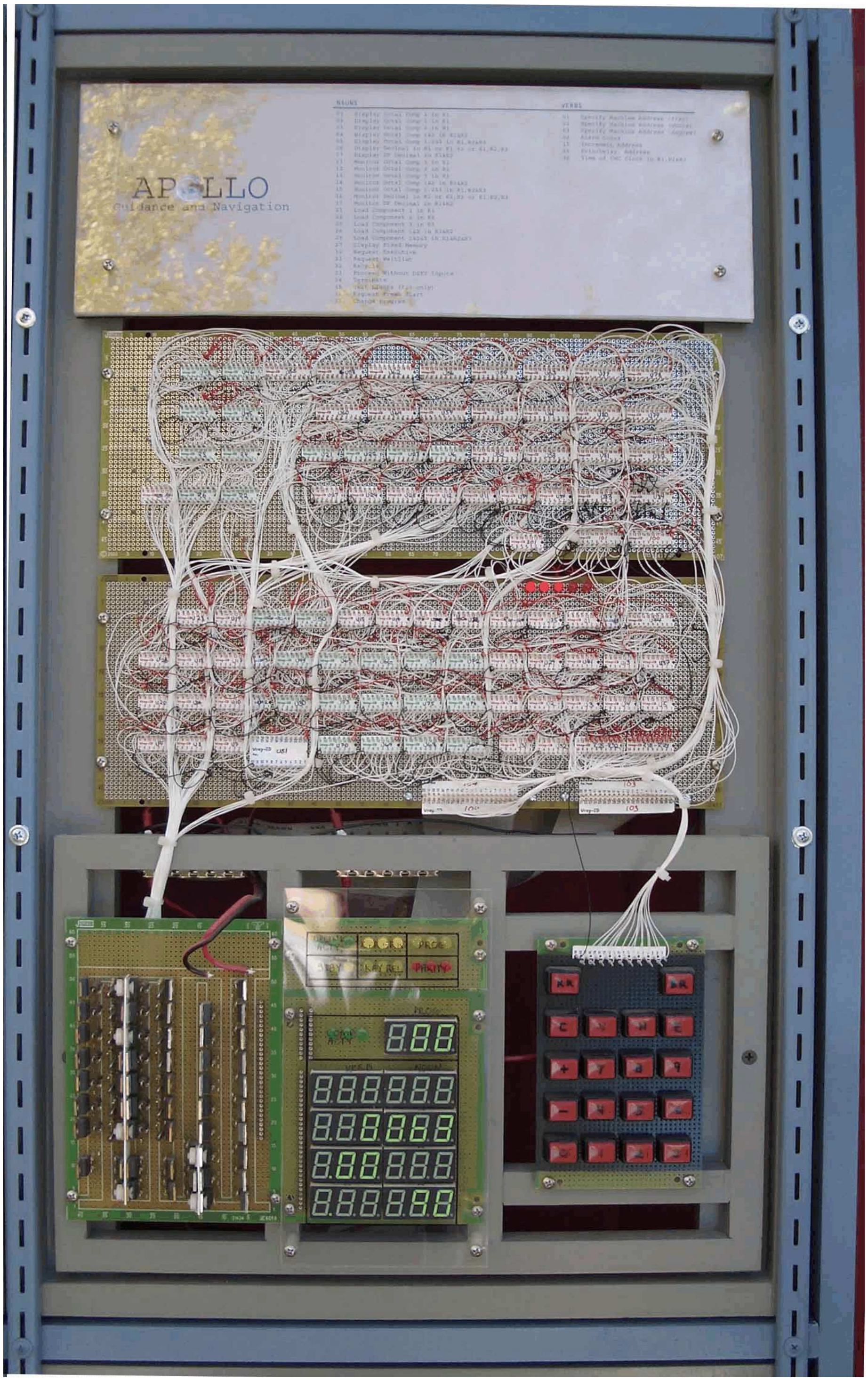
Part 7 C++ Simulator: A low-level simulator that runs assembled AGC code.

Part 8 Flight Software: My translation of portions of the COLOSSUS 249 flight software.

Part 9 Test & Checkout: A suite of test programs in AGC assembly language.

Overview

The I/O Module (IO) has 5 subsystems: IMI, KBD, INP, OUT, DSP



IMI (I/O Module external Interface)
The IMI interfaces the I/O module to other AGC modules. 40-pin IDE connectors interface to the PROC and CTL modules. A 1-pin connector interfaces to the MEM module. Inputs taken those modules are buffered to 1 LSTTL load.

KBD (Keyboard)
An 18-button keyboard; the AGC's flight software user input interface. The keyboard/display unit is called the DSKY.

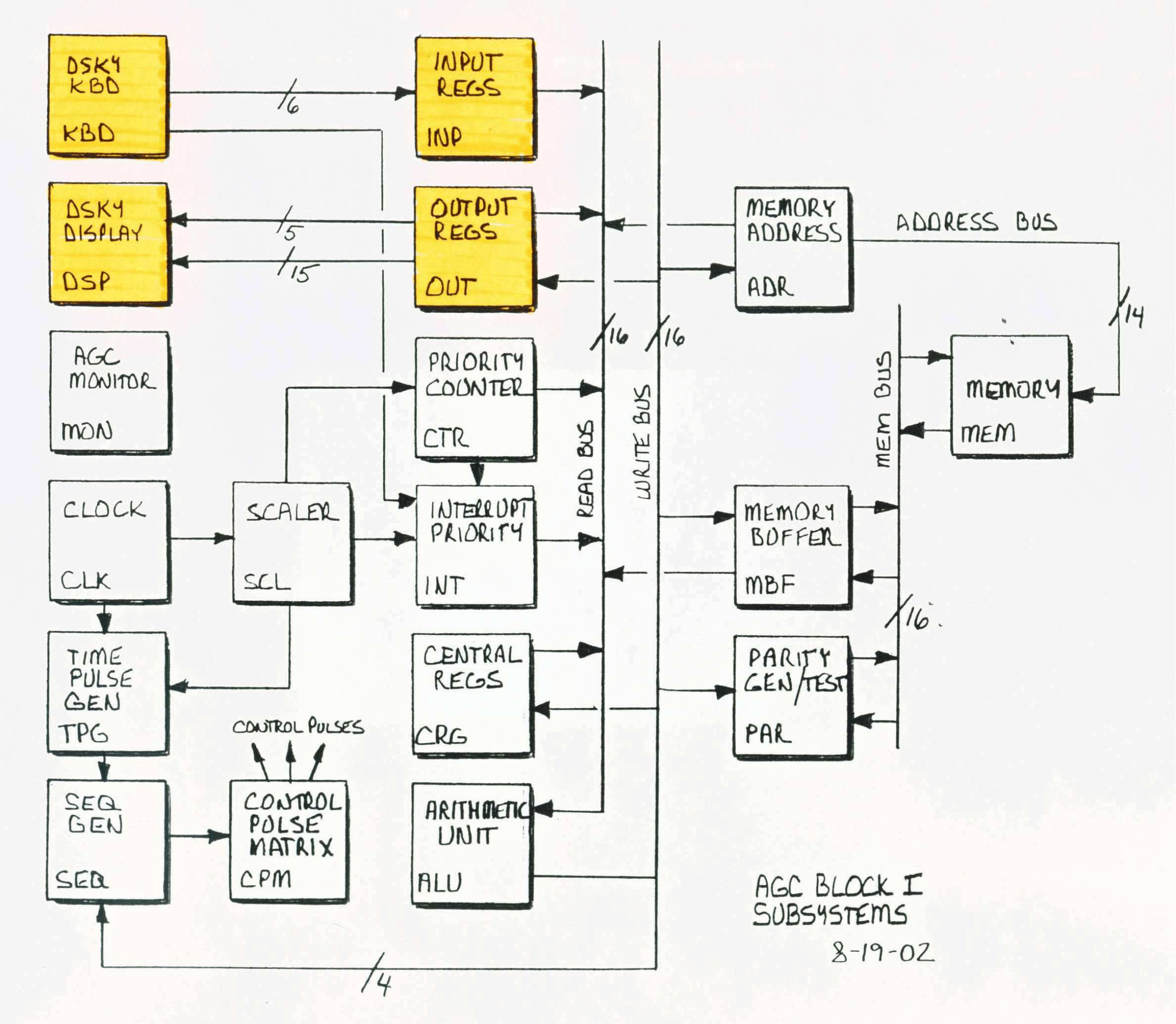
INP (Input Registers)
The AGC has 4 16-bit input registers that receive data from the keyboard and discrete logic signals. IN0 reads from the keyboard and the STANDBY ALLOWED discrete signal. IN1-IN3 are not implemented in this replica.

OUT (Output Registers)
The AGC has 5 16-bit output registers that drive the DSKY display and other spacecraft subsystems. OUT0 writes to the DSKY display; OUT1 drives the 6 discrete indicator lamps on the AGC DSKY display; OUT2-OUT4 are not implemented in this replica.

DSP (Display)

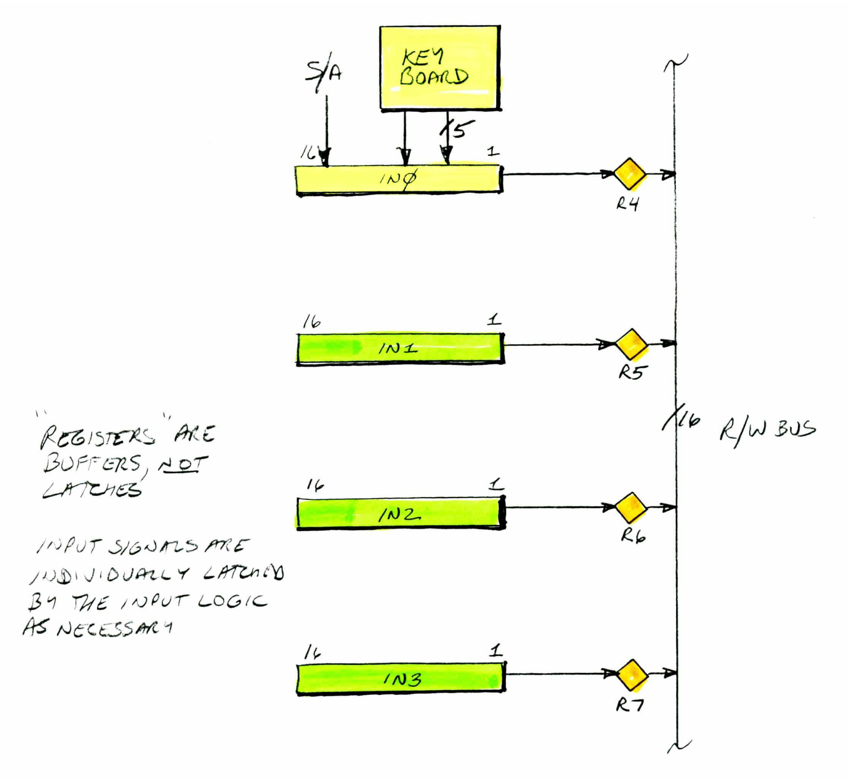
A matrix of green 7-segment displays; the output side of the AGC’s flight software user interface. There are (3) 5-digit displays with +/- signs which can display decimal or octal data, and (3) 2-digit displays to show the current program (PROG), verb, and noun.

An additional panel of 6 indicator lamps shows AGC status and alarm states.



AGC input registers and control signals that read them onto the bus are shown in the diagram to the right. The 5-bit keyboard code and STANDBY ALLOWED switch are read from “register 0" (IN0) when the R4 (RA4) control pulse is asserted. The signal is R4 because the register is mapped to memory address 4. The registers are actually buffers, not latches. Keyboard codes are latched internally in the keyboard subsystem.

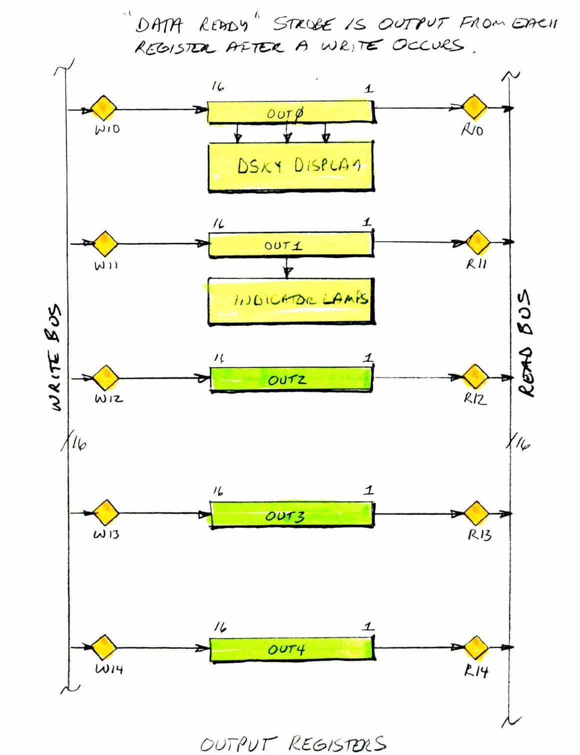
The IN1, IN2, and IN3 registers are not implemented in this replica.


S/A
KEY BOARD
5
16
1
IN∅
R4
16
1
IN1
R5
16
R/W BUS
"REGISTERS" ARE BUFFERS, NOT LATCHES
16
1
IN2
R6
INPUT SIGNALS ARE INDIVIDUALLY LATCHED BY THE INPUT LOGIC AS NECESSARY
16
1
IN3
R7

AGC output registers are shown in the next figure. OUT0 drives the 7-segment DSKY displays. W10 (WA10) loads data from the write bus into the DSKY display; the “10" is because it is mapped onto memory location 10 (octal). Each 16-bit word controls 2 digits on the display. The digit pair is selected by a 4-bit code at the top of the word.

OUT1 drives discrete indicator lamps on a panel adjacent to the 7-segment display. W11 (WA11) writes to the register, and R11 (RA11) reads from it.

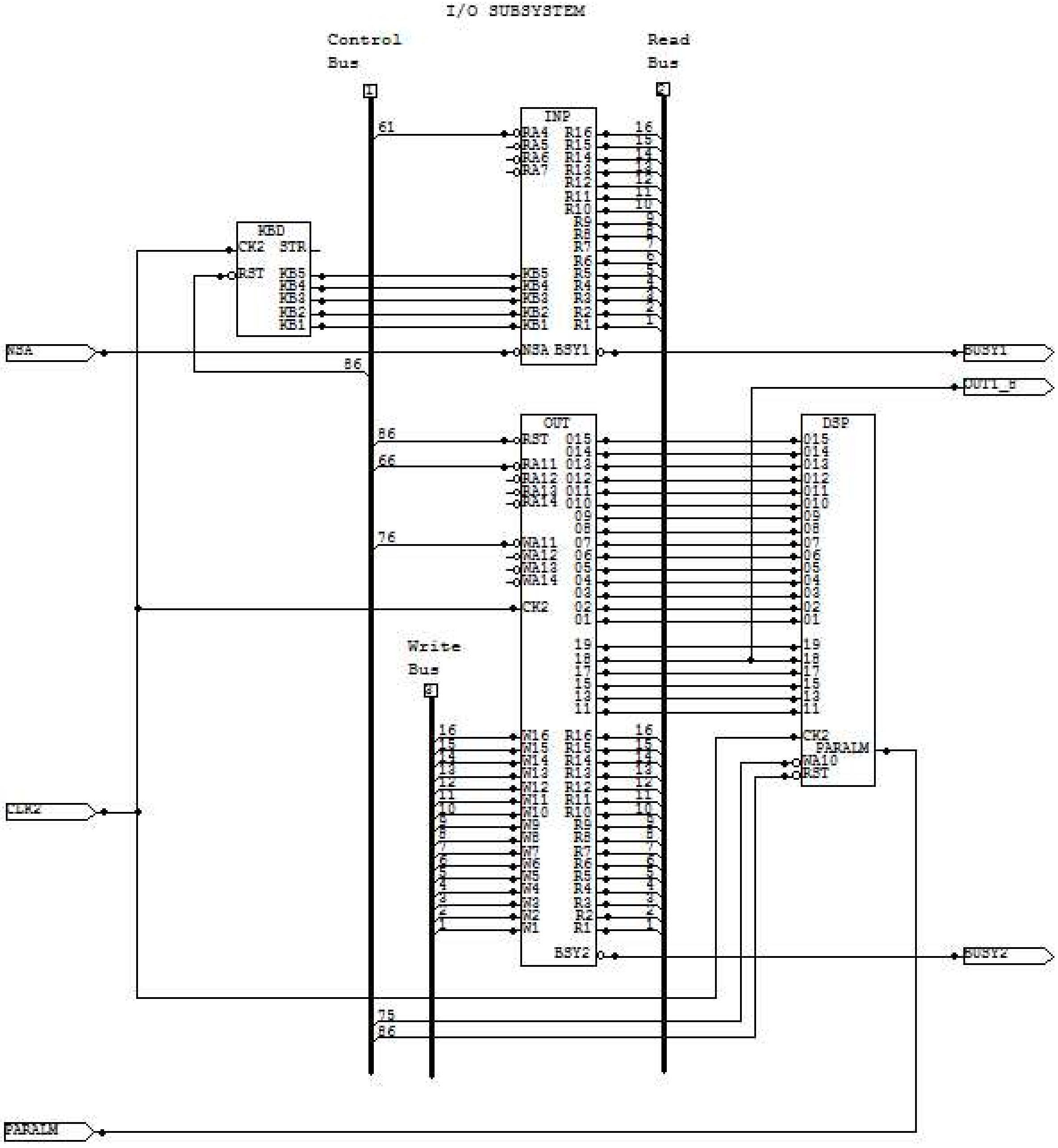
The OUT2, OUT3, and OUT4 registers are not implemented in this replica.



OUTPUT REGISTERS

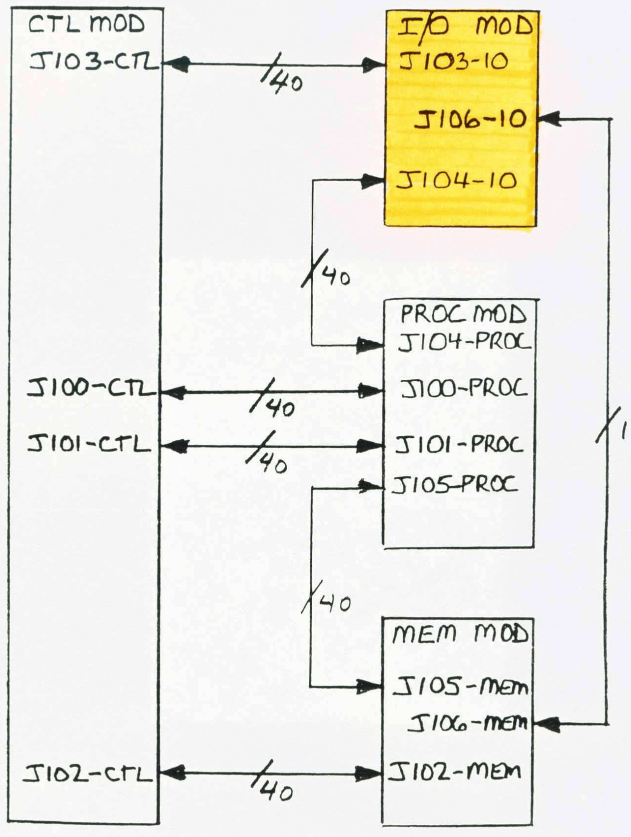
IO Internal Subsystem Interconnections

This diagram shows internal interconnections for the subsystems in the IO module.



IO Module External Interfaces

The IO module interfaces to the CTL and PROC modules through 40-pin IDE ribbon cables.



AGC MODULE INTERCONNECTIONS

J103-IO: CTL-to-I/O I/F

INPUTS (to IO):

PIN	signal	full name	state definition
1	CLK1	CLOCK1	1.024 MHz AGC clock phase 2 (normally low)
2	CLK2	CLOCK2	1.024 MHz AGC clock phase 2 (normally low)
3	NSA	STANDBY ALLOWED	0=standby allowed
5	GENRST	GENERAL RESET (86)	0=clear the DSKY, OUT1, and OUT2.
6	WA11	WRITE OUT1 (76)	0=write into OUT1 from write bus
7	WA10	WRITE OUT0 (75)	0=write into OUT0 (DSKY) from write bus
8	RA11	READ OUT1 (66)	0=output OUT1 register to read bus
9	RA4	READ IN0 (61)	0=output IN0 register to read bus
20	STBY	STANDBY	0=AGC is in the standby state

OUTPUTS (from IO):

PIN	signal	full name	state definition
40	OUT1_8	STANDBY ENABLED	1=standby enabled; works with STANDBY ALLOWED switch

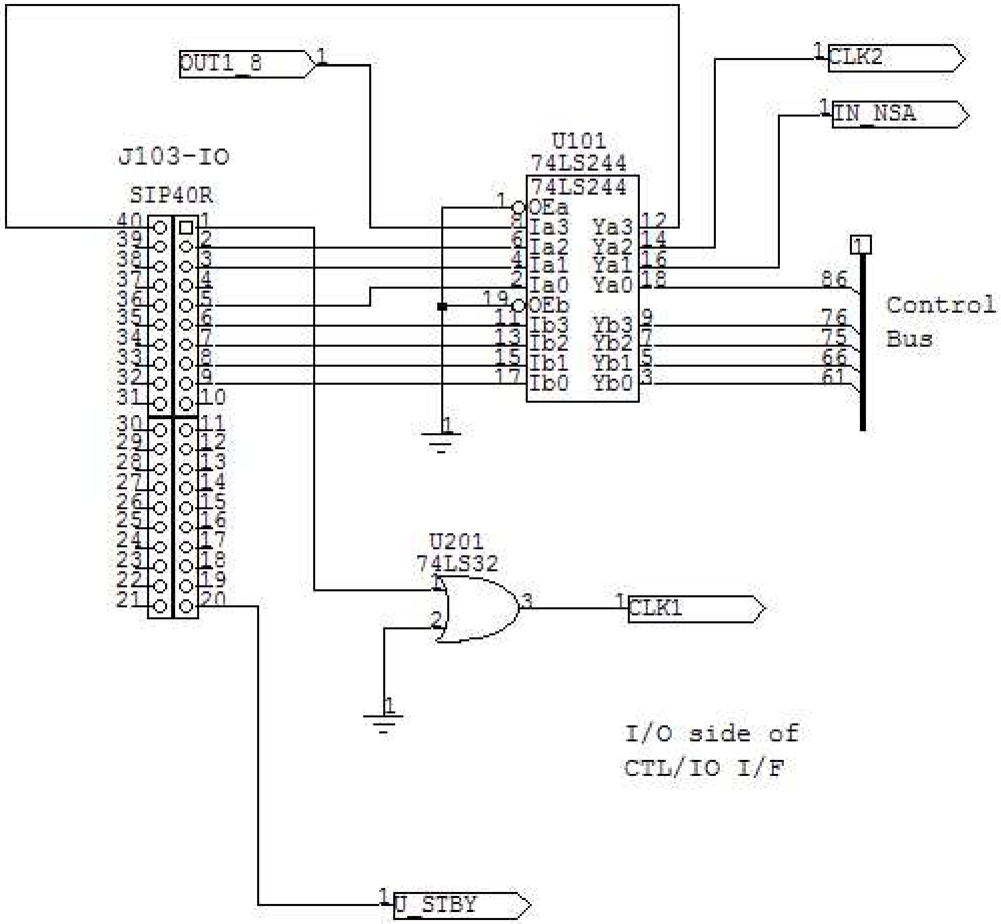
J104-IO: PROC-to-IO I/F

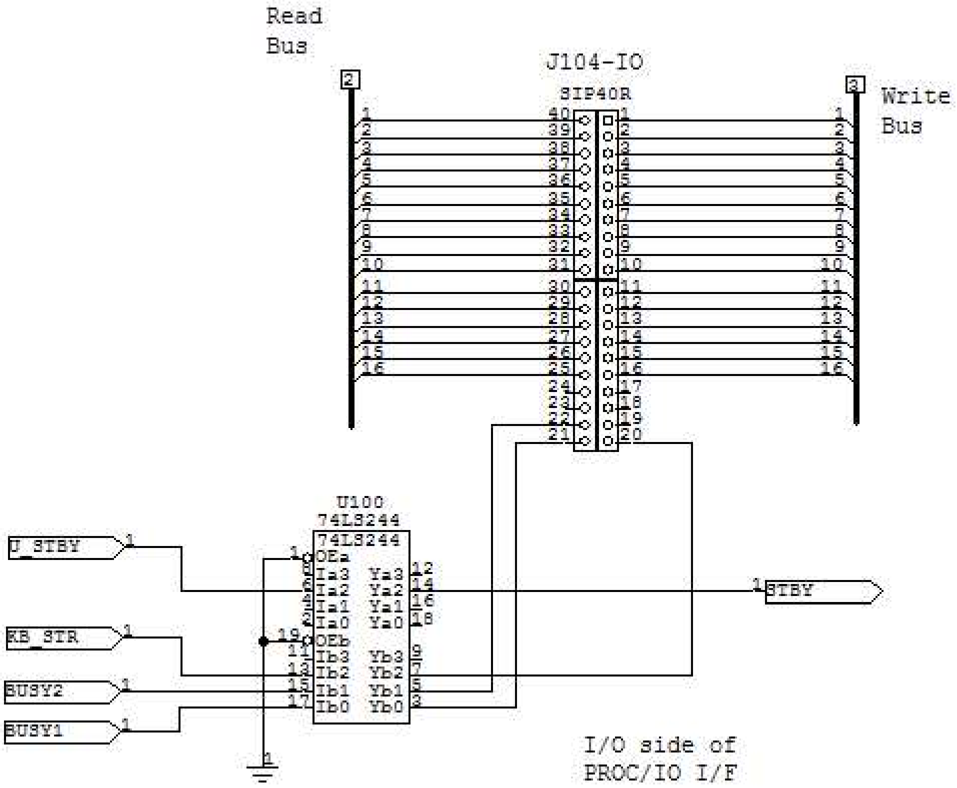
INPUTS (to IO):

PIN	signal	full name	state definition
1	WB_01	WRITE BUS 01	(lsb)
2	WB_02	WRITE BUS 02	
3	WB_03	WRITE BUS 03	
4	WB_04	WRITE BUS 04	
5	WB_05	WRITE BUS 05	
6	WB_06	WRITE BUS 06	
7	WB_07	WRITE BUS 07	
8	WB_08	WRITE BUS 08	
9	WB_09	WRITE BUS 09	
10	WB_10	WRITE BUS 10	
11	WB_11	WRITE BUS 11	
12	WB_12	WRITE BUS 12	
13	WB_13	WRITE BUS 13	
14	WB_14	WRITE BUS 14	
15	WB_15	WRITE BUS 15	US (overflow) bit
16	WB_16	WRITE BUS 16	SG (sign) bit

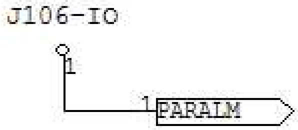
OUTPUTS (from IO):

PIN	signal	full name	state definition
40	RB_01	READ BUS 01	(lsb)
39	RB_02	READ BUS 02	
38	RB_03	READ BUS 03	
37	RB_04	READ BUS 04	
36	RB_05	READ BUS 05	
35	RB_06	READ BUS 06	
34	RB_07	READ BUS 07	
33	RB_08	READ BUS 08	
32	RB_09	READ BUS 09	
31	RB_10	READ BUS 10	
30	RB_11	READ BUS 11	
29	RB_12	READ BUS 12	
28	RB_13	READ BUS 13	
27	RB_14	READ BUS 14	
26	RB_15	READ BUS 15	US (overflow) bit
25	RB_16	READ BUS 16	SG (sign) bit
22	BUSY2	READ BUS BUSY	0=OUT registers output to read bus
21	BUSY1	READ BUS BUSY	0=INP registers output to read bus
20	KB_STR	KEY STROBE	1=key pressed strobe; to KEYRUPT. Key data is valid on the negative edge of KB_STR. Data is latched until the next keypress.


OUT1_8
CLK2
IN_NSA
J103-IO
SIP40R
U101
74LS244
74LS244
OEa
Ia3
Ia2
Ia1
Ia0
OEb
Ib3
Ib2
Ib1
Ib0
Ya3
Ya2
Ya1
Ya0
Yb3
Yb2
Yb1
Yb0
Control
Bus
86
76
75
66
61
U201
74LS32
CLK1
J_STBY
I/O side of
CTL/IO I/F



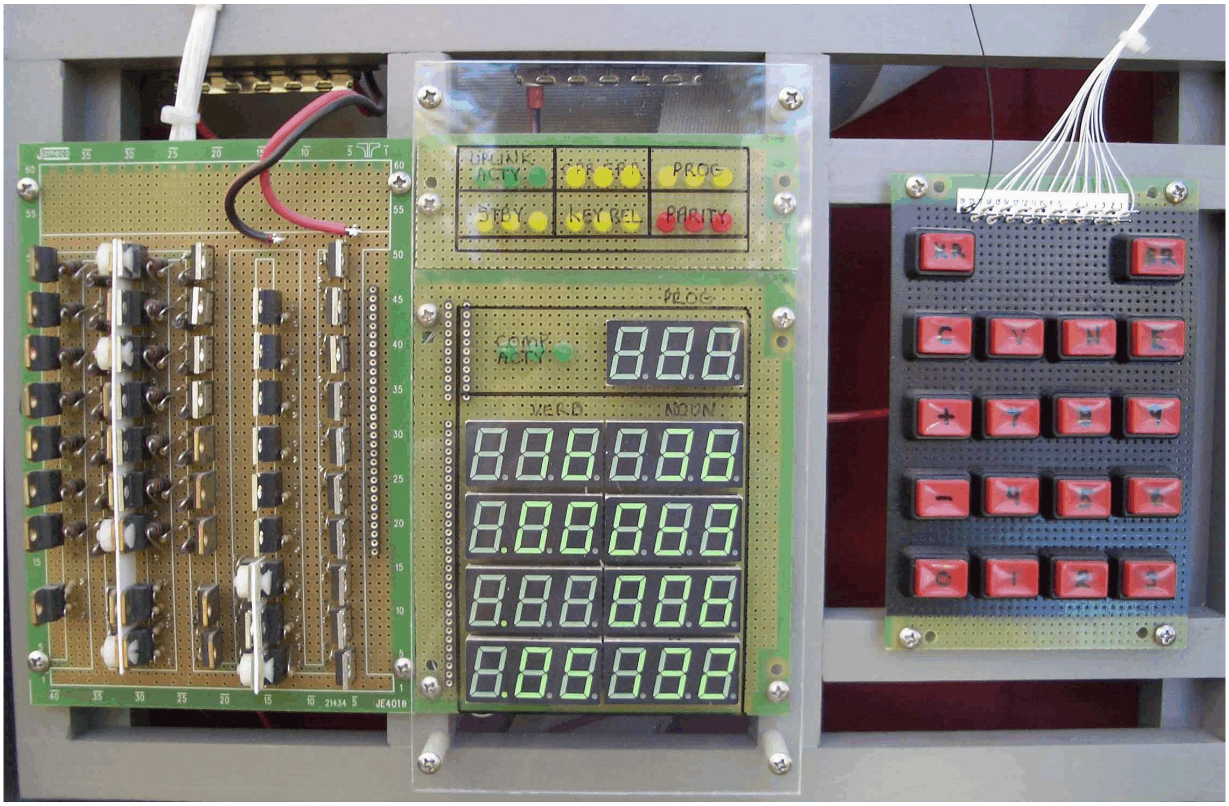
I/O side of
PROC/IO I/F



I/O side of
MEM/IO I/F

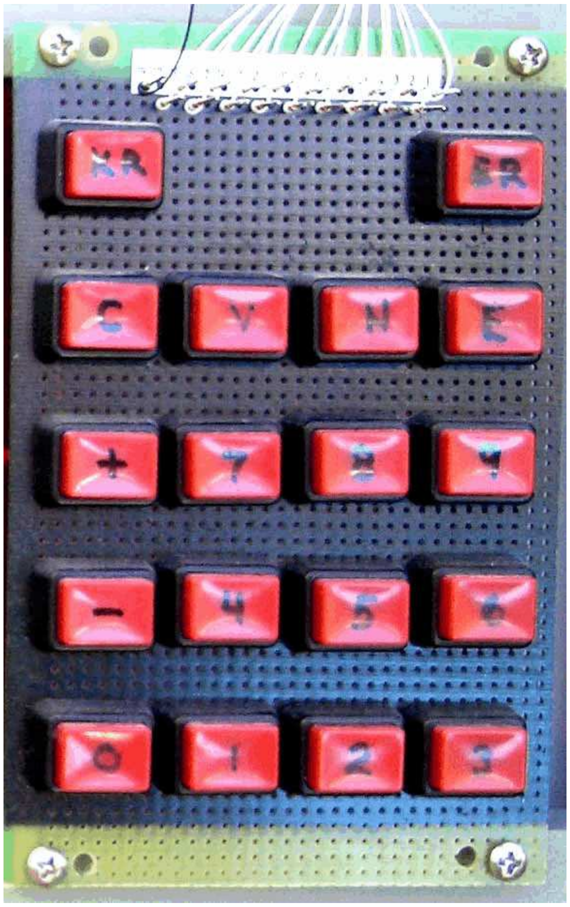
IO DISPLAY/KEYBOARD (DSKY)

The keyboard/display portion of the IO module contains a keyboard, a bank of 7-segment displays, a panel of discrete indicator lamps, and a board of display drivers.



DSKY KEYBOARD

The DSKY has an 18-button keyboard:



0-9 Decimal (or octal) digits.

+ Plus sign for decimal entries.

- Minus sign for decimal entries.

VERB Tells the AGC the next 2 digits entered will be a VERB.

NOUN Tells the AGC the next 2 digits entered will be a NOUN.

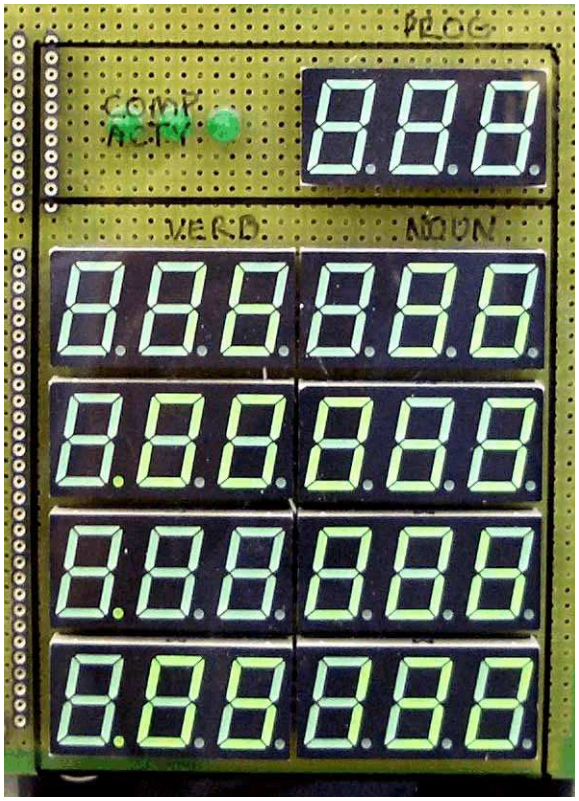
ENTER Tells the AGC the data entry is finished.

CLEAR Clears an error in entry.

ERR RST Resets the OPR ERR alarm lamp.

KEY REL Tells the AGC it can have control of the display. If the AGC wants control of the display, the KEL REL lamp will be flashing.

DSKY 7-SEGMENT DISPLAY



COMP ACTY A green indicator lamp that illuminates when the AGC is not idle. The lamp is controlled by the “dummy job”, the lowest priority job in the AGC EXEC software’s non-preemptive multitasking. When the dummy job is running, the lamp is extinguished because the AGC is idle. When the dummy job exits because there is a higher priority job running, the lamp illuminates. The light is driven by bit 1 of OUT1.

PROG The 2-digit code for the current AGC program. Driven by OUT0.

VERB The 2-digit code for the selected VERB. Verbs are actions; directives for the AGC to do something, such as loading or displaying memory data. Driven by OUT0.

NOUN The 2-digit code for the selected NOUN. The noun is the thing acted upon by the verb. Nouns usually refer to memory locations, which are mapped to some AGC function. Driven by OUT0.

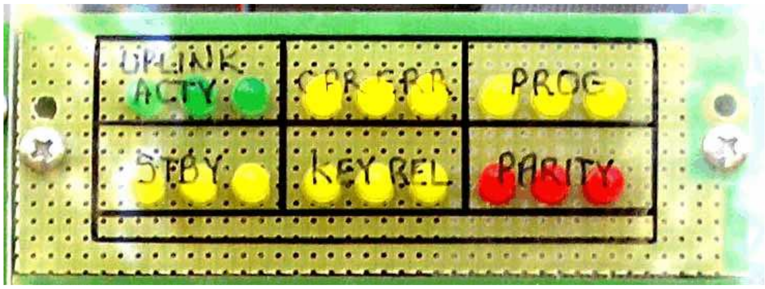
R1 Register 1. The uppermost of the three 5-digit displays. Registers R1, R2, and R3 can display data in octal or decimal. Octal data is displayed without a sign. Decimal data is indicated by the presence of a + or - sign in front of the data. The displays I used in my replica cannot display a + sign, so I modified the logic slightly: decimal data is represented by a leftmost decimal point. Negative decimal numbers have a - sign and the decimal point; positive numbers just have the decimal point. Driven by OUT0.

R2 Register 2. The middle of the three 5-digit displays. Driven by OUT0.

R3 Register 3. The bottommost of the three 5-digit displays. Driven by OUT0.

IO DISCRETE INDICATORS

The DSKY has a panel of discrete indicator lamps (LEDs) to show status or caution and warning signals. Four of the lamps are driven by bits in output register 1 (OUT1). The parity alarm is driven by a signal from the MEM module. The standby lamp is driven by the standby state of the time pulse generator (TPG) in the CTL module.



UPLINK ACTY
Uplink activity. Illuminates when data is uplinked to the AGC. Driven by bit 3 (UPTL) of OUT1.

OPR ERR
Operator Error (also called CHECK FAIL). Illuminates when the AGC detects a data entry error. Driven by bit 7 of OUT1.

KEY REL
Key Release. Illuminated by the AGC when it needs to use the display, but the operator has taken control of it. The AGC causes this lamp to flash to signal the operator to release control of the display by hitting the KEY REL button. Driven by bit 5 (KEY RELS) of OUT1.

PROG
Program Alarm. Illuminates when the AGC encounters an error condition. Driven by bit 8 of OUT1.

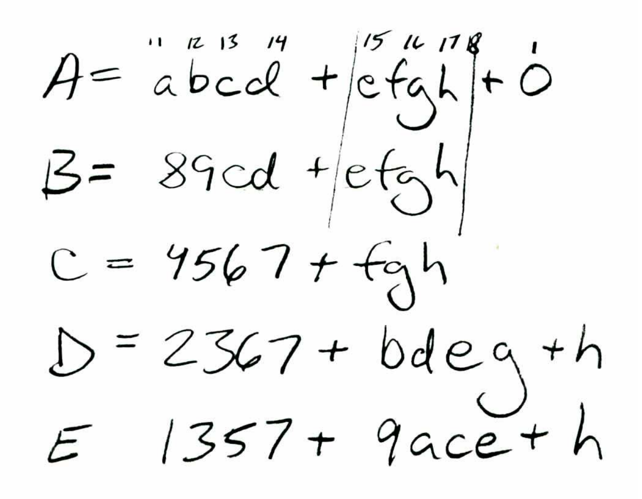
STBY
Standby. Illuminates when the AGC is in the STANDBY mode.

PARITY ALARM
Illuminates when a parity error is detected during the memory cycle in the MEM module.

KBD (Keyboard)

The keyboard is an 18-pushbutton unit that generates and latches a 5-bit code. The code is given in “Keyboard and Display System Program for AGC (Program Sunrise)”, A. I. Green and J. J. Rocchio, E-1574, MIT Instrumentation Laboratory, Cambridge, MA, 1964.

The keyboard codes and logic for generating the 5-bit signal is reproduced to the right. The “Key Name” column identifies the name of the keyboard key; “A” through “E” are the 5 logic signals for the 5-bit code, where “A” is the MSB.



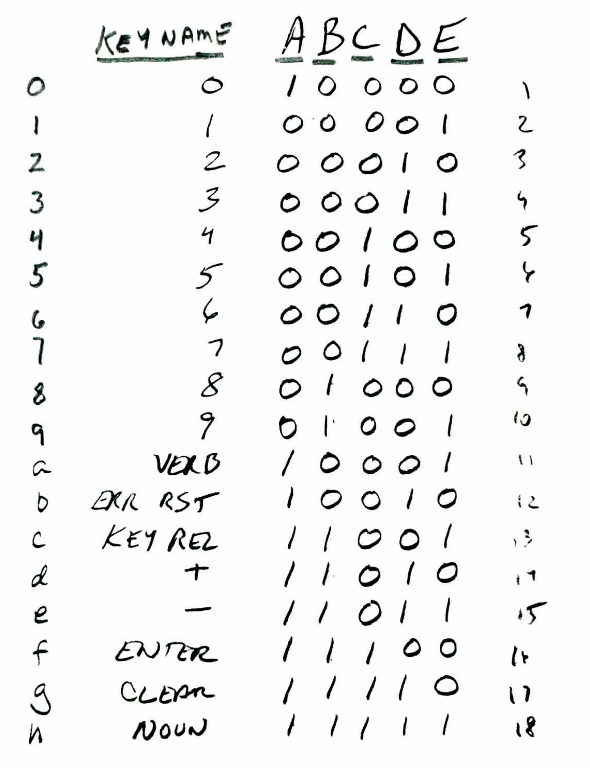
$$A = \overset{11}{a}\overset{12}{b}\overset{13}{c}\overset{14}{d} + \overset{15}{e}\overset{16}{f}\overset{17}{g}\overset{18}{h} + \overset{1}{0}$$

$$B = 89cd + efgh$$

$$C = 4567 + fgh$$

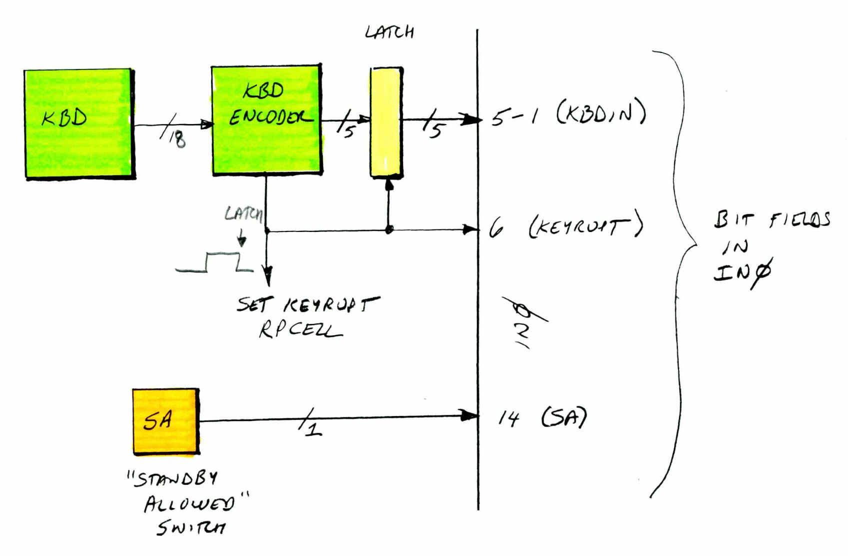
$$D = 2367 + bdeg + h$$

$$E \quad 1357 + 9ace + h$$



	KEY NAME	A	B	C	D	E	
0	0	1	0	0	0	0	1
1	1	0	0	0	0	1	2
2	2	0	0	0	1	0	3
3	3	0	0	0	1	1	4
4	4	0	0	1	0	0	5
5	5	0	0	1	0	1	6
6	6	0	0	1	1	0	7
7	7	0	0	1	1	1	8
8	8	0	1	0	0	0	9
9	9	0	1	0	0	1	10
a	VERB	1	0	0	0	1	11
b	ERR RST	1	0	0	1	0	12
c	KEY REL	1	1	0	0	1	13
d	+	1	1	0	1	0	14
e	−	1	1	0	1	1	15
f	ENTER	1	1	1	0	0	16
g	CLEAR	1	1	1	1	0	17
h	NOUN	1	1	1	1	1	18

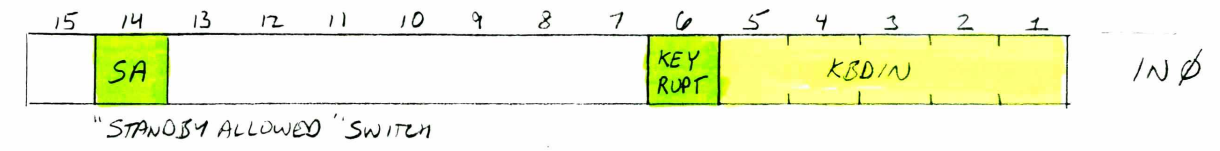
The 18 switches in the keyboard feed into the combinational logic encoder which generates the 5-bit signal. The output of the encoder feeds into a 5-bit latch.



The keys are debounced by generating a “keypress” signal whenever a key is pushed. The keypress signal feeds through a “D” flip-flop clocked at around 100Hz. This samples the keypress signal every 10 mSec and latches the sample. The 10 mSec interval exceeds the contact bounce time of the keyboard switches.

To give the combinational logic time to settle before the keycode is latched, the output of the keypress D flip-flop is fed into an RC monstable. Latching occurs on the trailing edge of the one-shot pulse.

The keyboard codes are fed into “input register” IN0, which is really just a buffer that gates the codes onto the read bus when the proper read signal is asserted. The original design also maps the keypress strobe which generates the keyboard interrupt (KEYRUPT) onto bit 6 of the register, but I skipped this since there doesn’t seem to be any practical reason for doing it and the COLOSSUS flight software doesn’t seem to look at the field.

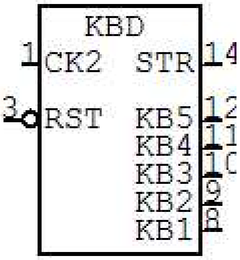


The STANDBY ALLOWED switch (CTL module) maps to be 14.

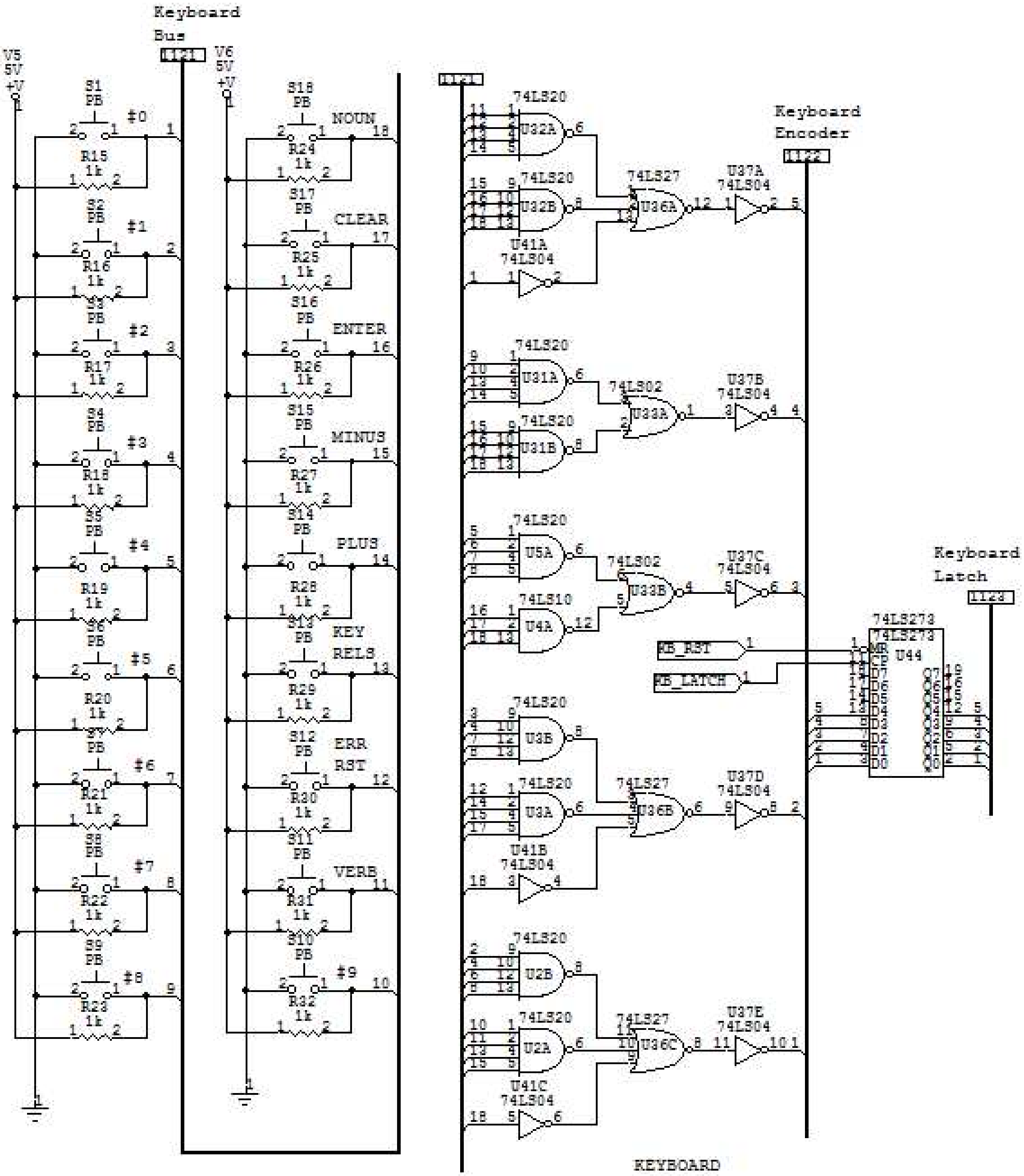
KBD INPUTS:

I/F	signal	full name	state definition
CLK:			
	CLK2	CLOCK 2	data transfer occurs on falling edge
CPM:			
	GENRST	GENERAL RESET	0=reset KBD register

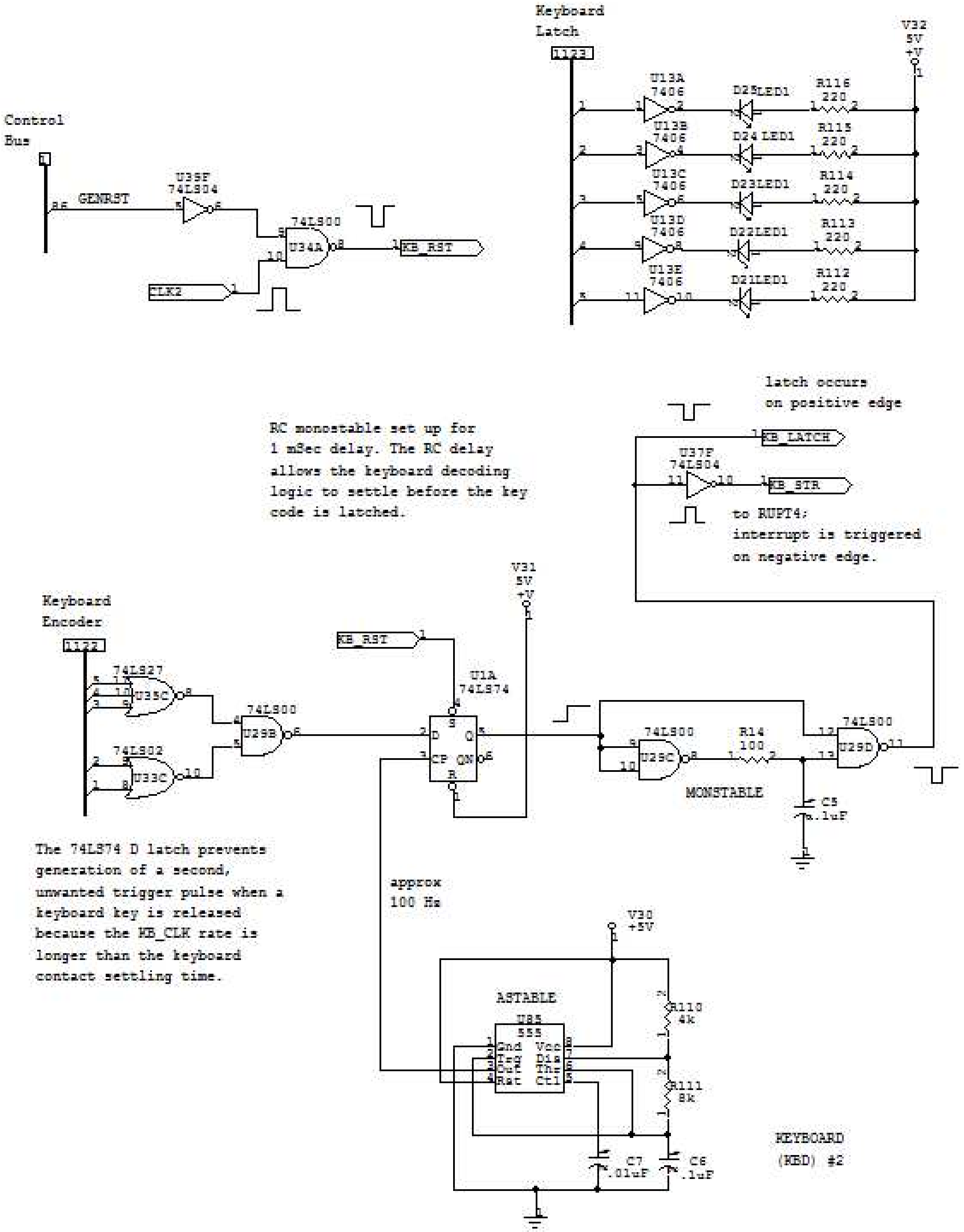
KBD OUTPUTS:



I/F	signal	full name	state definition
KBD:			
	KB_01	KEYBOARD BUS 01	Keyboard codes
	...		
	KB_05	KEYBOARD BUS 05	
INT:			
	KB_STR	KEY STROBE	1=key pressed strobe; to KEYRUPT. Key data is valid on the negative edge of KB_STR. Data is latched until the next keypress.



KEYBOARD
(KBD) #1



RC monostable set up for 1 mSec delay. The RC delay allows the keyboard decoding logic to settle before the key code is latched.

latch occurs on positive edge

to RUPT4; interrupt is triggered on negative edge.

The 74LS74 D latch prevents generation of a second, unwanted trigger pulse when a keyboard key is released because the KB_CLK rate is longer than the keyboard contact settling time.

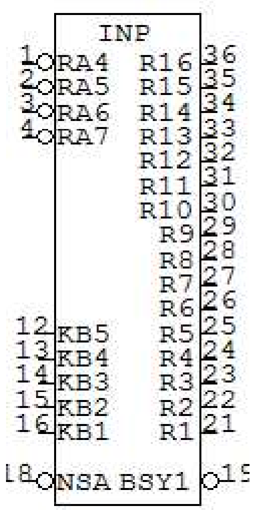
approx 100 Hz

KEYBOARD (KBD) #2

INP (Input Registers)

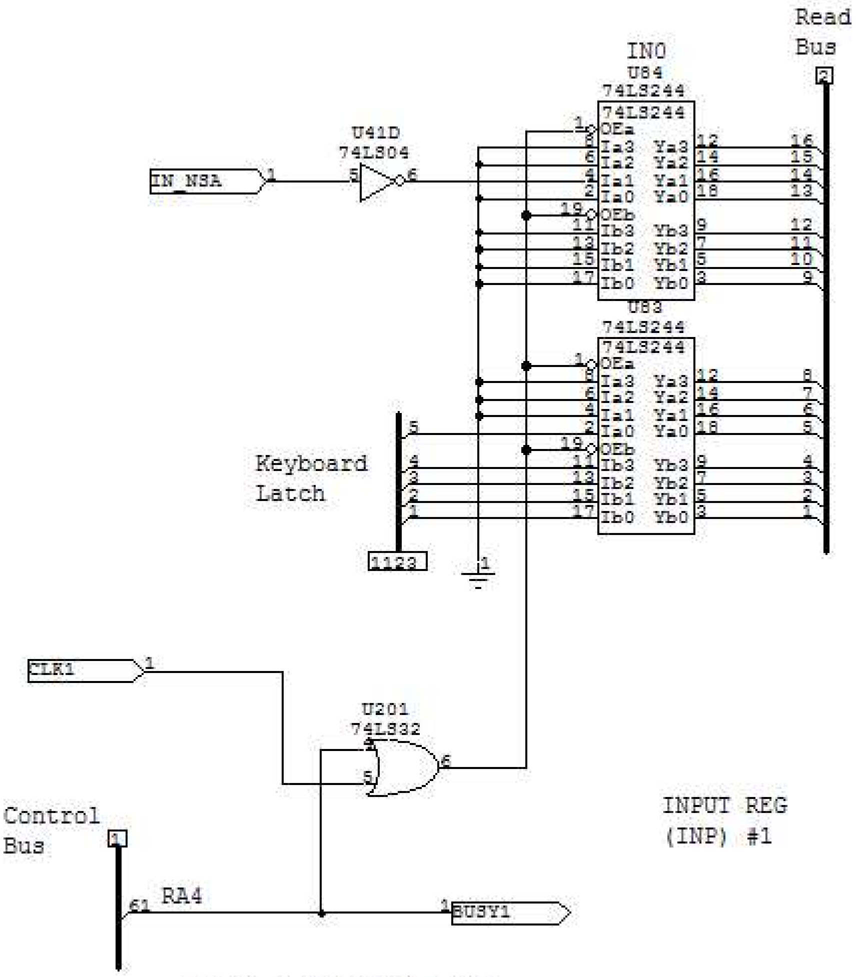
INP INPUTS:

I/F	signal	full name	state definition
CPM:			
	RA4	READ IN0	0=output IN0 register to read bus
	RA5	READ IN1	0=output IN1 register to read bus
	RA6	READ IN2	0=output IN2 register to read bus
	RA7	READ IN3	0=output IN3 register to read bus
KBD:			
	KB_01	KEYBOARD BUS 01	
	...		
	KB_05	KEYBOARD BUS 05	
	NSA	STANDBY ALLOWED	0=standby allowed



INP OUTPUTS:

I/F	signal	full name	state definition
RBUS:			
	RB_01	READ BUS 01	
	...		
	RB_14	READ BUS 14	
	RB_15	READ BUS 15	US (overflow) bit for read/write bus
	RB_16	READ BUS 16	SG (sign) bit for read/write bus
	BUSY	READ BUS BUSY	0=output enabled to read bus



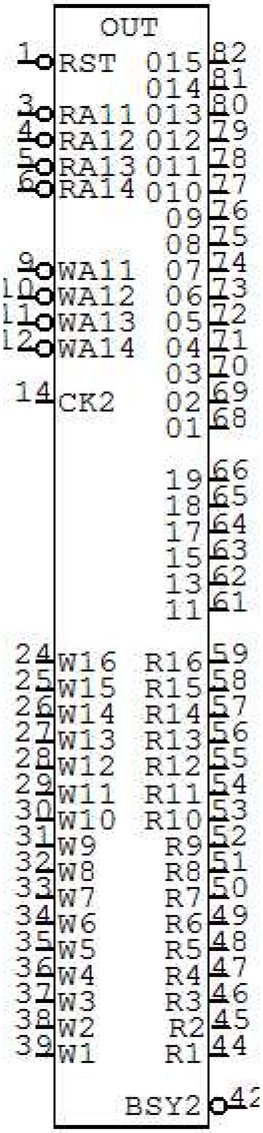
INPUT REG
(INP) #1

Note: inputs IN1, IN2,
and IN3 are not currently
implemented.

OUT (Output Registers)

OUT INPUTS:

I/F	signal	full name	state definition
CLK:			
	CLK2	CLOCK 2	data transfer occurs on falling edge
CPM:			
	RA11	READ OUT1	0=OUT1 to read bus
	RA12	READ OUT2	0=OUT2 to read bus
	RA13	READ OUT3	0=OUT3 to read bus
	RA14	READ OUT4	0=OUT4 to read bus
	WA11	WRITE OUT1	0=load OUT1 from write bus
	WA12	WRITE OUT2	0=load OUT2 from write bus
	WA13	WRITE OUT3	0=load OUT3 from write bus
	WA14	WRITE OUT4	0=load OUT4 from write bus
	GENRST	GENERAL RESET	0=clear DSKY, OUT1, and OUT2.
WBUS:			
	WB_01	WRITE BUS 01	
	...		
	WB_14	WRITE BUS 14	
	WB_15	WRITE BUS 15	US (overflow) bit for write bus
	WB_16	WRITE BUS 16	SG (sign) bit for write bus

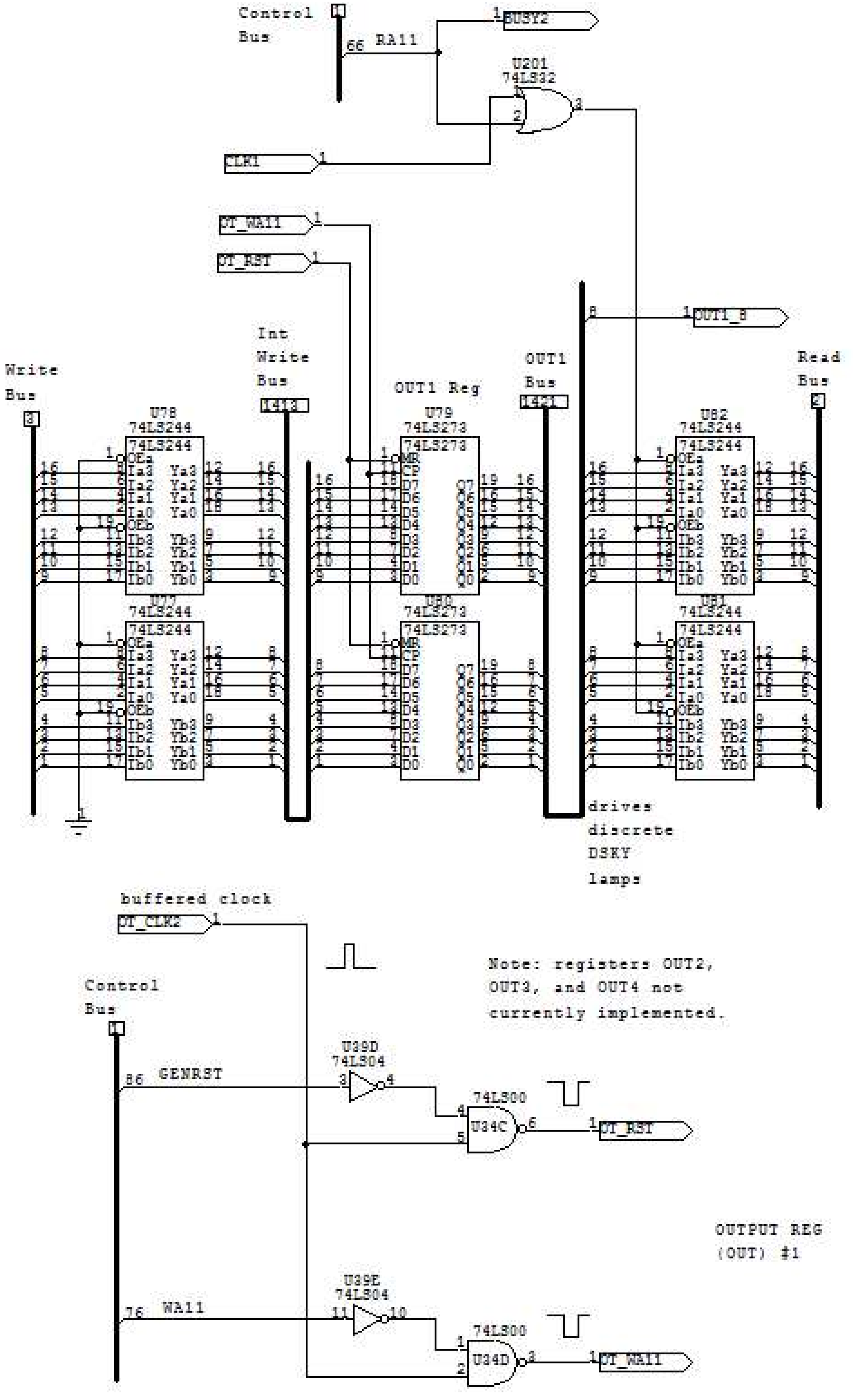


OUT OUTPUTS:

I/F	signal	full name	state definition
DSP:			
	OT0_01	OUT0 REG 01	OUT0 register output to DSKY
	...		
	OT0_16	OUT0 REG 16	
	OT1_01	OUT1 REG 01	COMP panel indicator; 1=on
	OT1_03	OUT1 REG 03	UPTL panel indicator; 1=on
	OT1_05	OUT1 REG 05	KEY RELS panel indicator; 1=on
	OT1_07	OUT1 REG 07	CHECK FAIL panel indicator 1=on
	OT1_08	OUT1 REG 08	STBY panel indicator 1=on
	OT1_09	OUT1 REG 09	PROG ALM panel indicator 1=on

RBUS:

RB_01	READ BUS 01	
...		
RB_14	READ BUS 14	
RB_15	READ BUS 15	US (overflow) bit for read/write bus
RB_16	READ BUS 16	SG (sign) bit for read/write bus
BUSY	READ BUS BUSY	0=output enabled to read bus

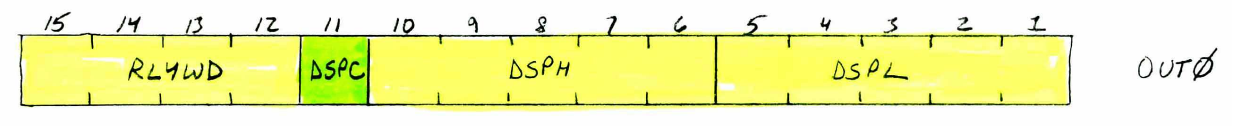


Note: registers OUT2, OUT3, and OUT4 not currently implemented.

OUTPUT REG (OUT) #1

DSP (Display)

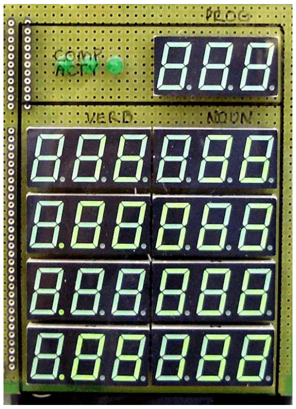
The 7-segment DSKY display is driven by output register 0 (OUT0). Each 16-bit write to OUT0 writes data to a pair of 7-segment digits.



Four fields in OUT0 are involved: The relay word (RLYWD; bits 12-15) field selects the pair of digits; the DSPH field (bits 6-10) contains the 5-bit numerical code for the left digit in the pair, and DPSL (bits 1-5) has the code for the right digit. The 1-bit DPSC (bit 11) field controls verb/noun flash (enables 1 Hz blinking of the VERB and NOUN digits) and the plus and minus signs to the left of the three 5-digit “registers” on the DSKY display.

Bits 15-12 RLYWD	Bit 11 DSPC	Bits 10-6 DSPH	Bits 5-1 DSPL
1011		MD1	MD2
1010	FLASH	VD1	VD2
1001		ND1	ND2
1000	UPACT		R1D1
0111	+R1S	R1D2	R1D3
0110	-R1S	R1D4	R1D5
0101	+R2S	R2D1	R2D2
0100	-R2S	R2D3	R2D4
0011		R2D5	R3D1
0010	+R3S	R3D2	R3D3
0001	-R3S	R3D4	R3D5

Each 7-segment digit on the display has a name (VD1, VD2, etc). The digits are physically arranged like this:



				MD1	MD2	: major mode (PROG)
VD1	VD2 : VERB			ND1	ND2	: NOUN
R1S	R1D1	R1D2	R1D3	R1D4	R1D5	: register 1
R2S	R2D1	R2D2	R2D3	R2D4	R2D5	: register 2
R3S	R3D1	R3D2	R3D3	R3D4	R3D5	: register 3

In my assembled unit, the displays were in groups of 3, so some digits were not needed and left unwired.

The 5-bit codes that illuminate each digit in the display are given below; these are the codes sent to the DPSH and DPSL fields in OUT0.

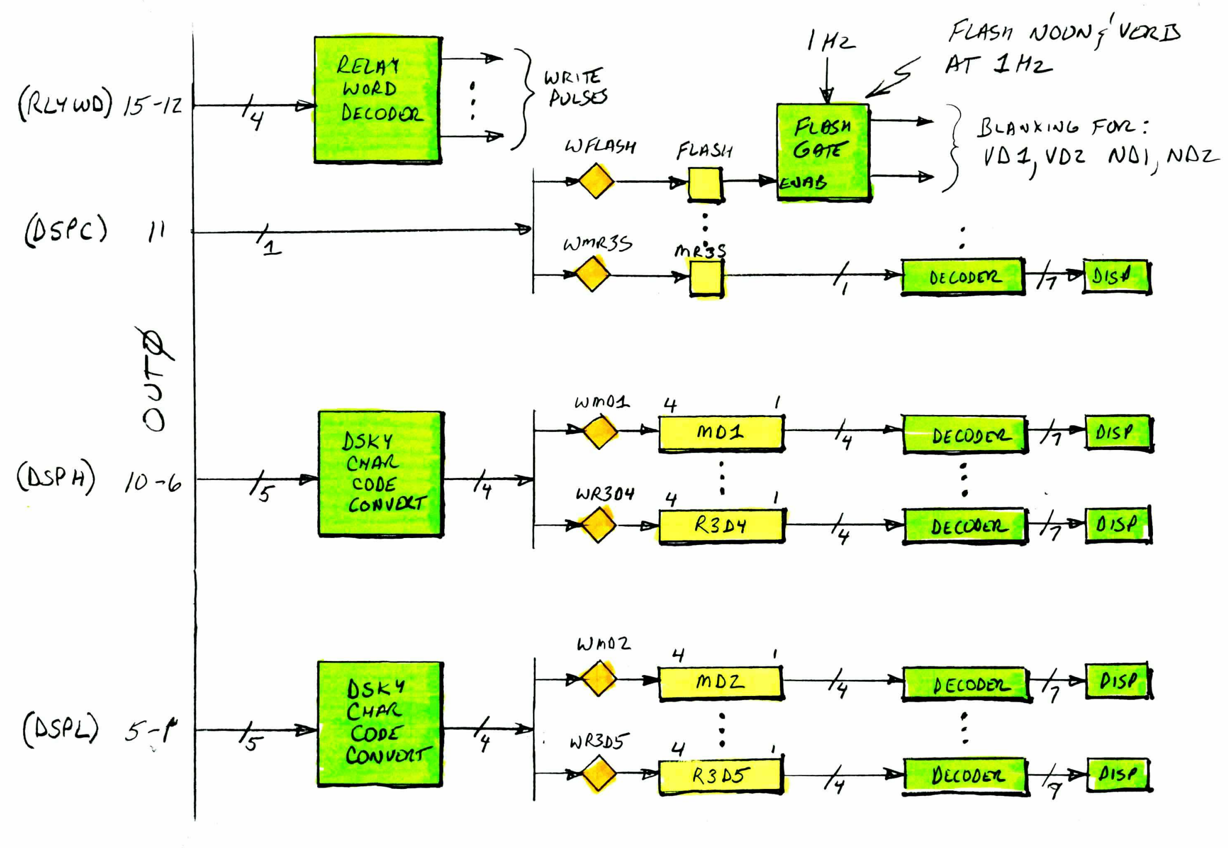
In my implementation, I translate them into 4-bit binary-coded decimal representation (BCD) and feed them into a 74LS47 7-segment decoder. The mapping of the AGC digit to my

74LS47 decoder code is also given. The AGC digit codes are very peculiar; I suspect they were chosen for easy decoding into the 7-segment displays.

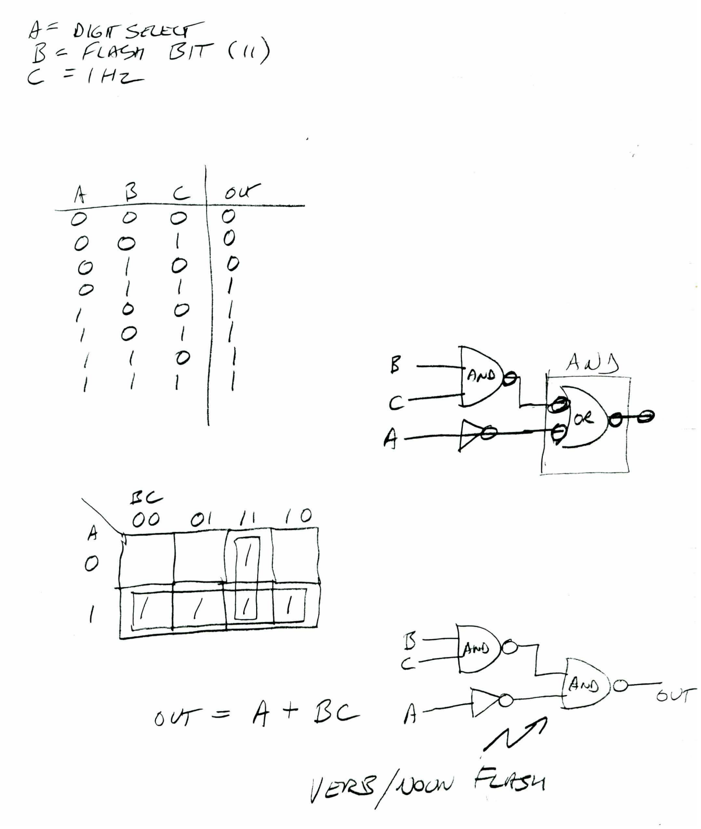
Digit	AGC	74LS47
Blank	00000	1111
0	10101	0000
1	00011	0001
2	11001	0010
3	11011	0011
4	01111	0100
5	11110	0101
6	11100	0110
7	10011	0111
8	11101	1000
9	11111	1001

My initial block diagram for the DSP logic is shown here. Two combinational logic code converters changes the 5-bit AGC code (DSPH, DPSL) into 4-bit BCD. The converted codes are latched into 4-bit registers by write pulses decoded by the relay word (RLYWD) decoder. Single bit latches hold the flash and sign bit codes transmitted by DSPC (bit 11 of OUT0).

Although I show separate decoders for each digit, I actually multiplexed the display to minimize the hardware. In this way, I only needed a pair of 74LS47 decoders; one for DSPH and the other for DSPL.



Some back-of-the-envelope bits and pieces of the logic design are also shown here. One “diagram” shows the verb/noun flash logic. Note the simple Karnaugh map (a graphical method for reducing boolean expressions), and a bit of bubble-pushing (a graphical technique for applying DeMorgan’s Theorem to transform logic functions between AND and OR).



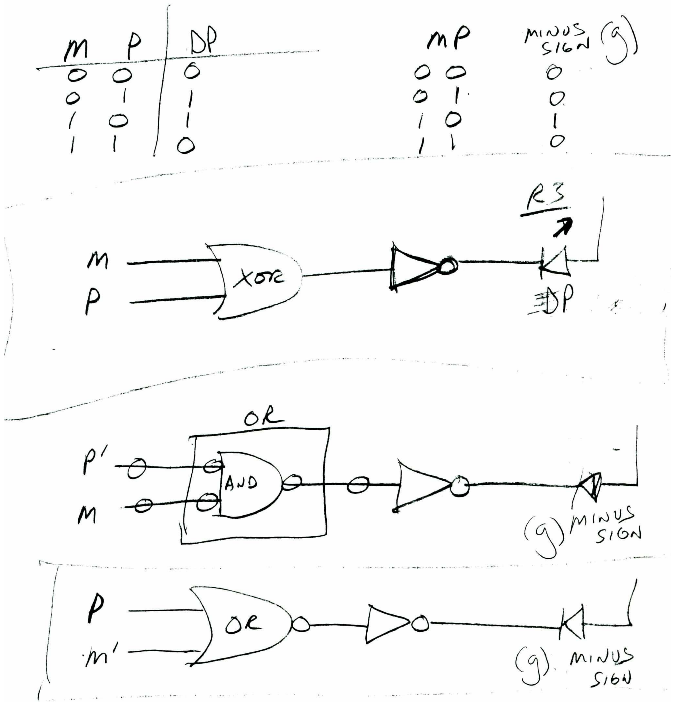
A= DIGIT SELECT
B = FLASH BIT (11)
C = 1 Hz

A	B	C	OUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

A \ BC	00	01	11	10
0			1	
1	1	1	1	1

OUT = A + BC

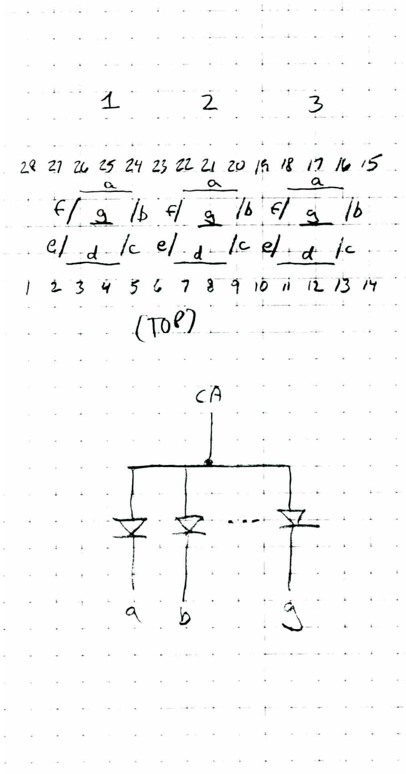
The other “diagram” shows the logic for the +/- signs on registers 1, 2, and 3. The displays I used in my replica cannot display a + sign, so I modified the AGC logic slightly: decimal data is represented by a leftmost decimal point. Negative decimal numbers have a - sign and decimal point; positive decimal numbers just have the decimal point.



M	P	DP
0	0	0
0	1	1
1	0	1
1	1	0

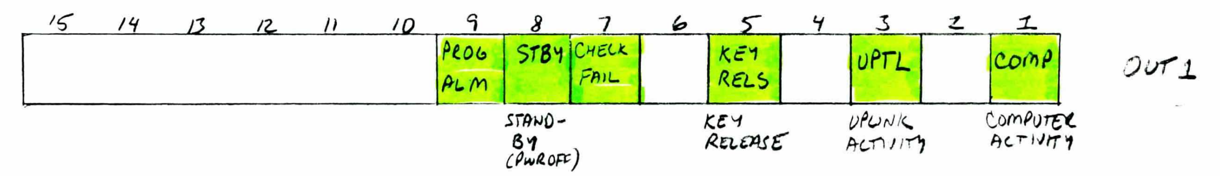
M	P	MINUS SIGN (g)
0	0	0
0	1	0
1	0	1
1	1	0

The digit display portion of the DSKY uses green common-anode LED displays grouped in three's. Like most components, these were purchased from JAMECO. Here's the pinouts:



1	1e
2	1d
3	DIGIT 1 CA
4	1c
5	1 d.p.
6	2e
7	2d
8	2c
9	2 dp
10	3e
11	3d
12	3g
13	3c
14	3 dp
15	3b
16	3a
17	3f
18	DIGIT 3 CA
19	DIGIT 2 CA
20	2b
21	2a
22	2g
23	2f
24	1b
25	1a
26	——
27	1f
28	1g

A panel of discrete indicator LEDs are mapped against bits in output register 1 (OUT1).

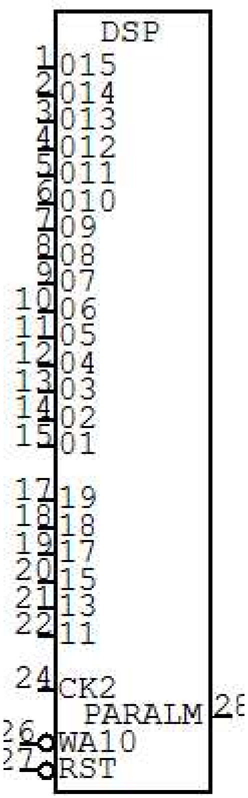


OUT1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
						PROG ALM	STBY	CHECK FAIL		KEY RELS		UPTL		COMP
							STAND-BY (PWROFF)			KEY RELEASE		UPLINK ACTIVITY		COMPUTER ACTIVITY

DSP INPUTS:

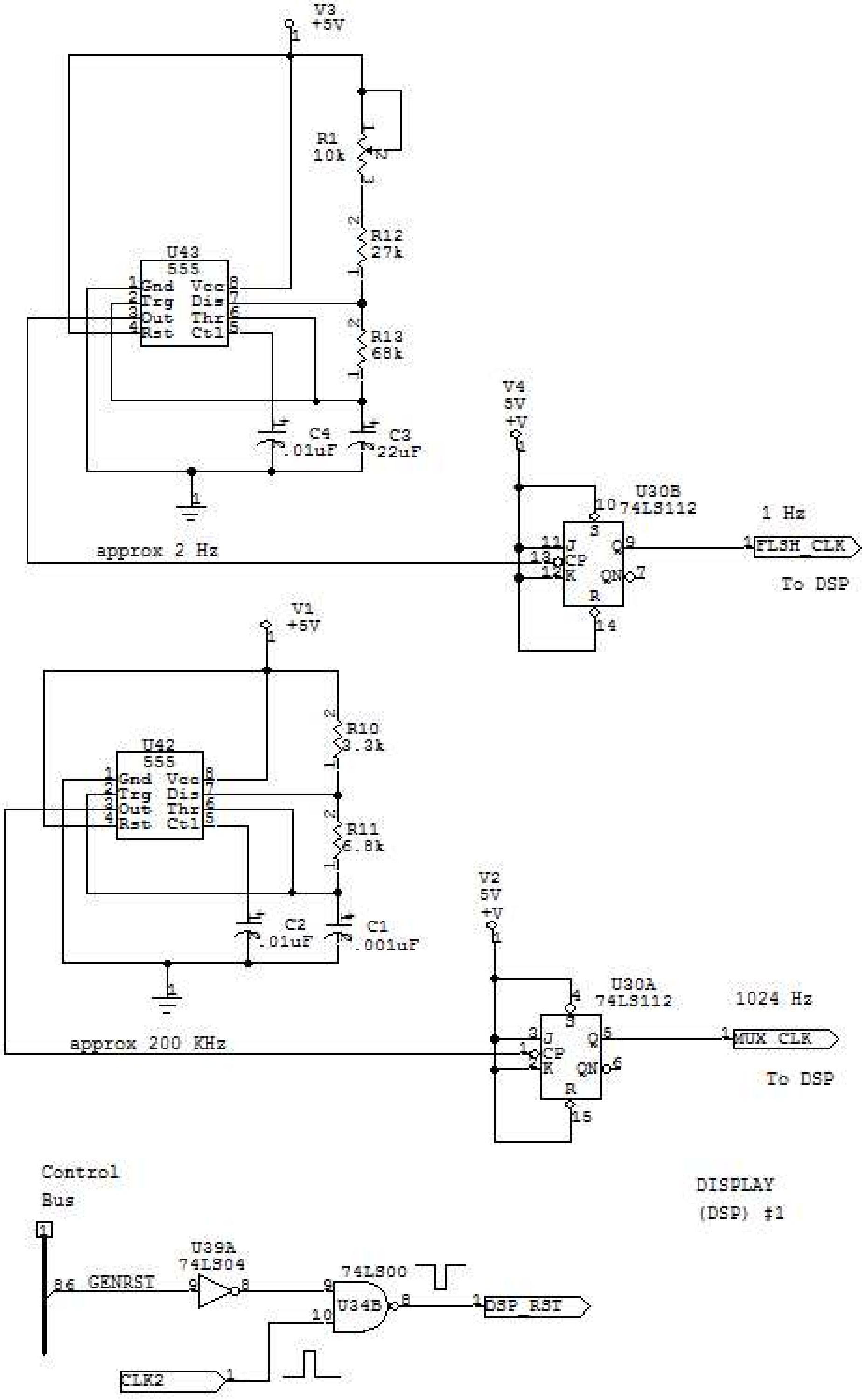
I/F	signal	full name	state definition
CLK:			
	CLK2	CLOCK 2	data transfer occurs on falling edge
PAR:			
	PARALM	PARITY ALARM	1=parity alarm
INP:			
	OT0_01	OUT0 REG 01	OUT0 register output to DSKY
	...		
	OT0_15	OUT0 REG 15	
	OT1_01	OUT1 REG 01	COMP panel indicator; 1=on
	OT1_03	OUT1 REG 03	UPTL panel indicator; 1=on
	OT1_05	OUT1 REG 05	KEY RELS panel indicator; 1=on
	OT1_07	OUT1 REG 07	CHECK FAIL panel indicator 1=on
	OT1_08	OUT1 REG 08	STBY panel indicator 1=on
	OT1_09	OUT1 REG 09	PROG ALM panel indicator 1=on
CPM:			
	WA10	WRITE OUT0	0=write into OUT0 (DSKY) from write bus
	GENRST	GENERAL RESET	0=clear the DSKY.

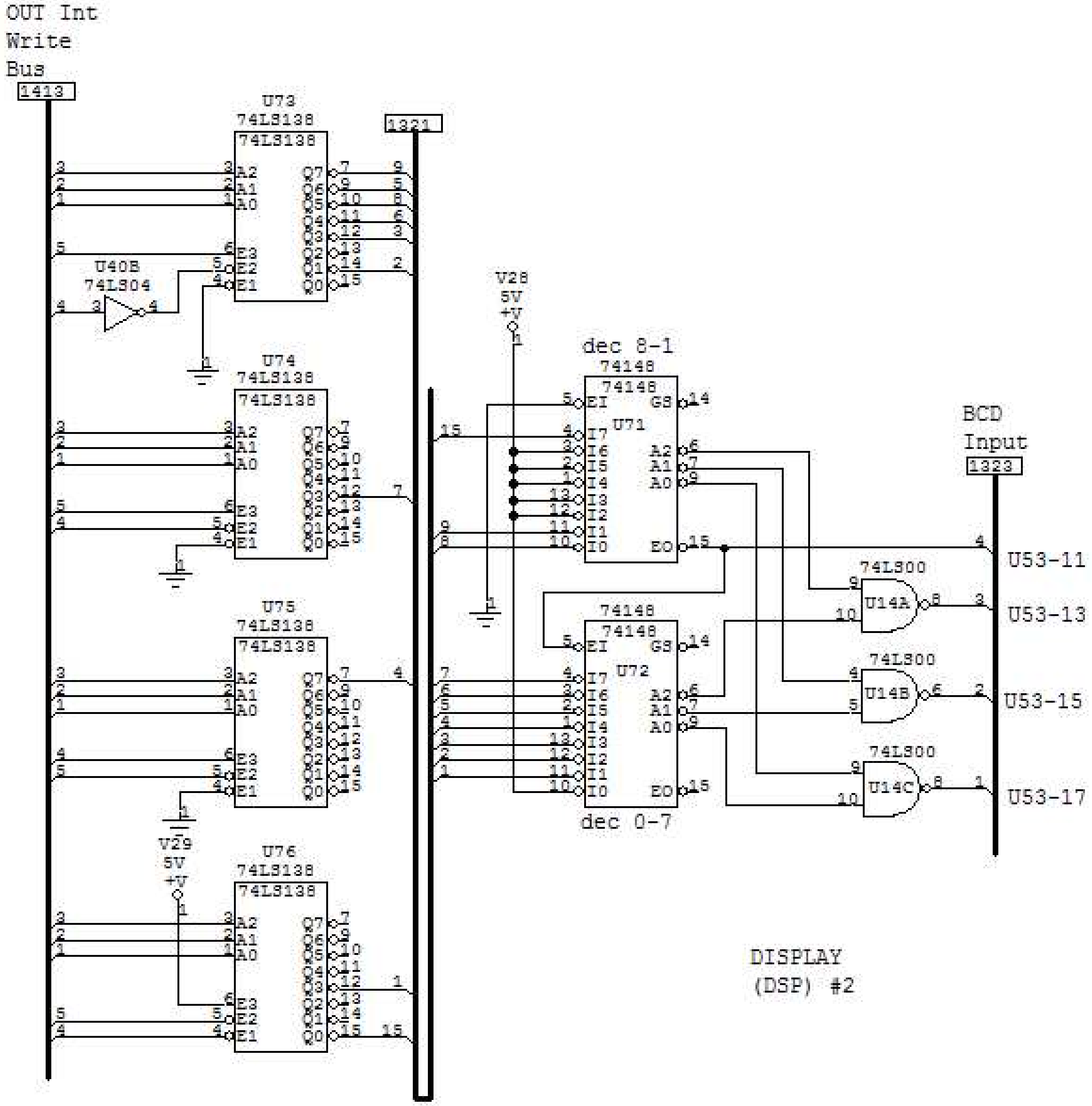


DSP OUTPUTS:

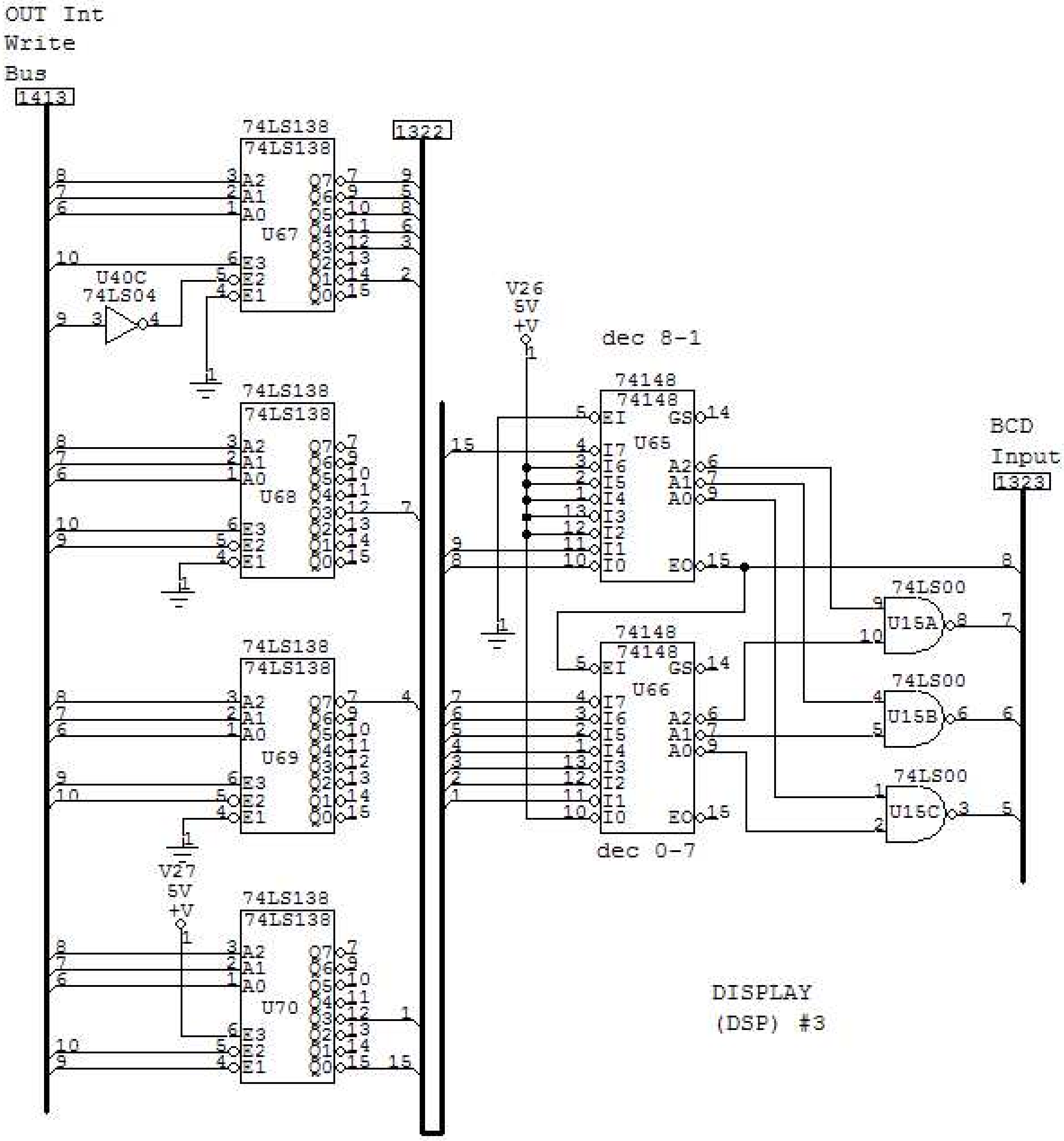
I/F	signal	full name	state definition

none.

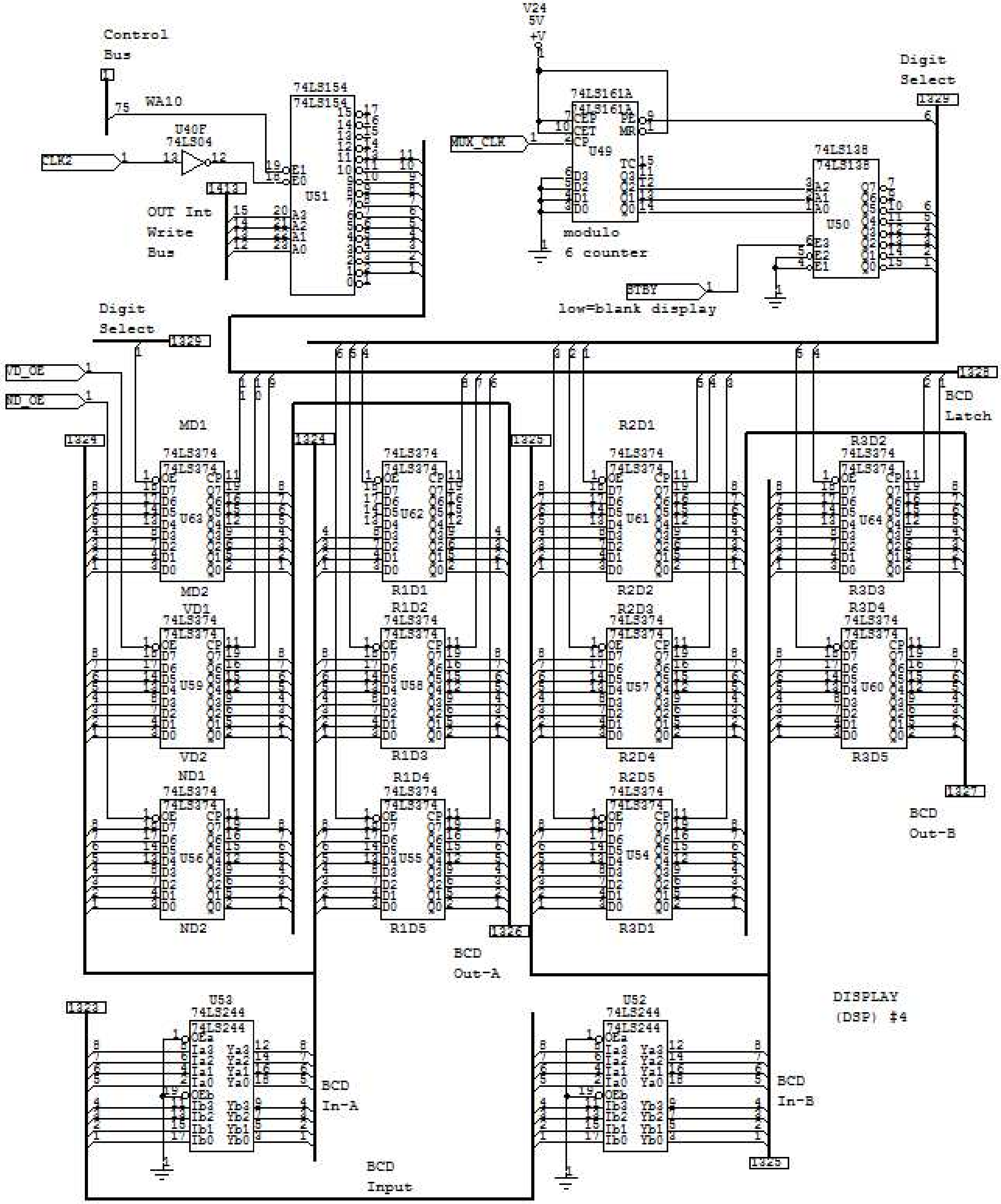

V3
+5V
R1
10k
R12
27k
R13
68k
U43
555
Gnd
Trg
Out
Rst
Vcc
Dis
Thr
Ctl
C4
.01uF
C3
22uF
approx 2 Hz
V4
5V
+V
U30B
74LS112
J
CP
K
Q
QN
S
R
1 Hz
FLSH_CLK
To DSP
V1
+5V
R10
3.3k
R11
6.8k
U42
555
Gnd
Trg
Out
Rst
Vcc
Dis
Thr
Ctl
C2
.01uF
C1
.001uF
approx 200 KHz
V2
5V
+V
U30A
74LS112
J
CP
K
Q
QN
S
R
1024 Hz
MUX_CLK
To DSP
Control
Bus
86 GENRST
U39A
74LS04
74LS00
U34B
DSP_RST
CLK2
DISPLAY
(DSP) #1



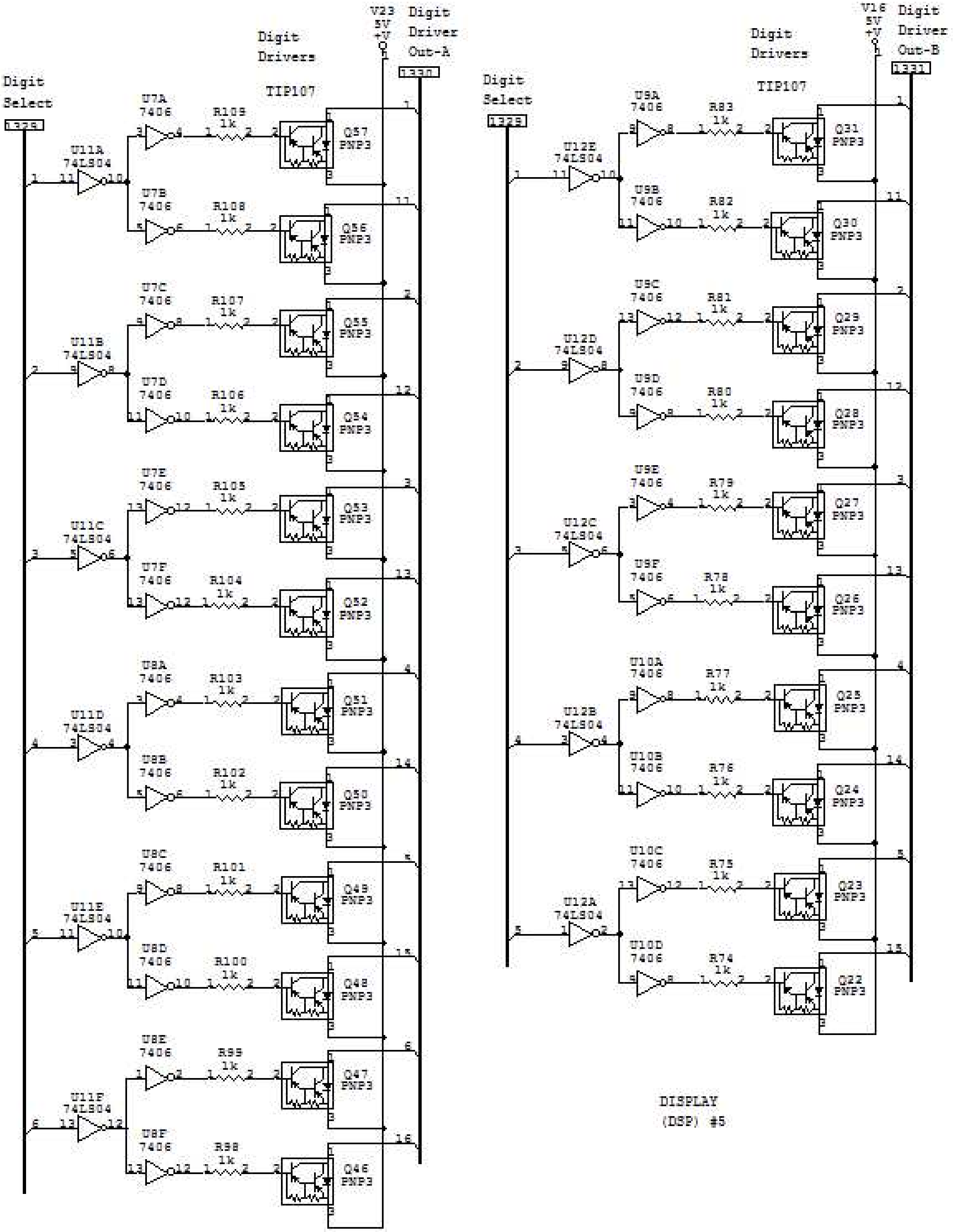
DISPLAY
(DSP) #2



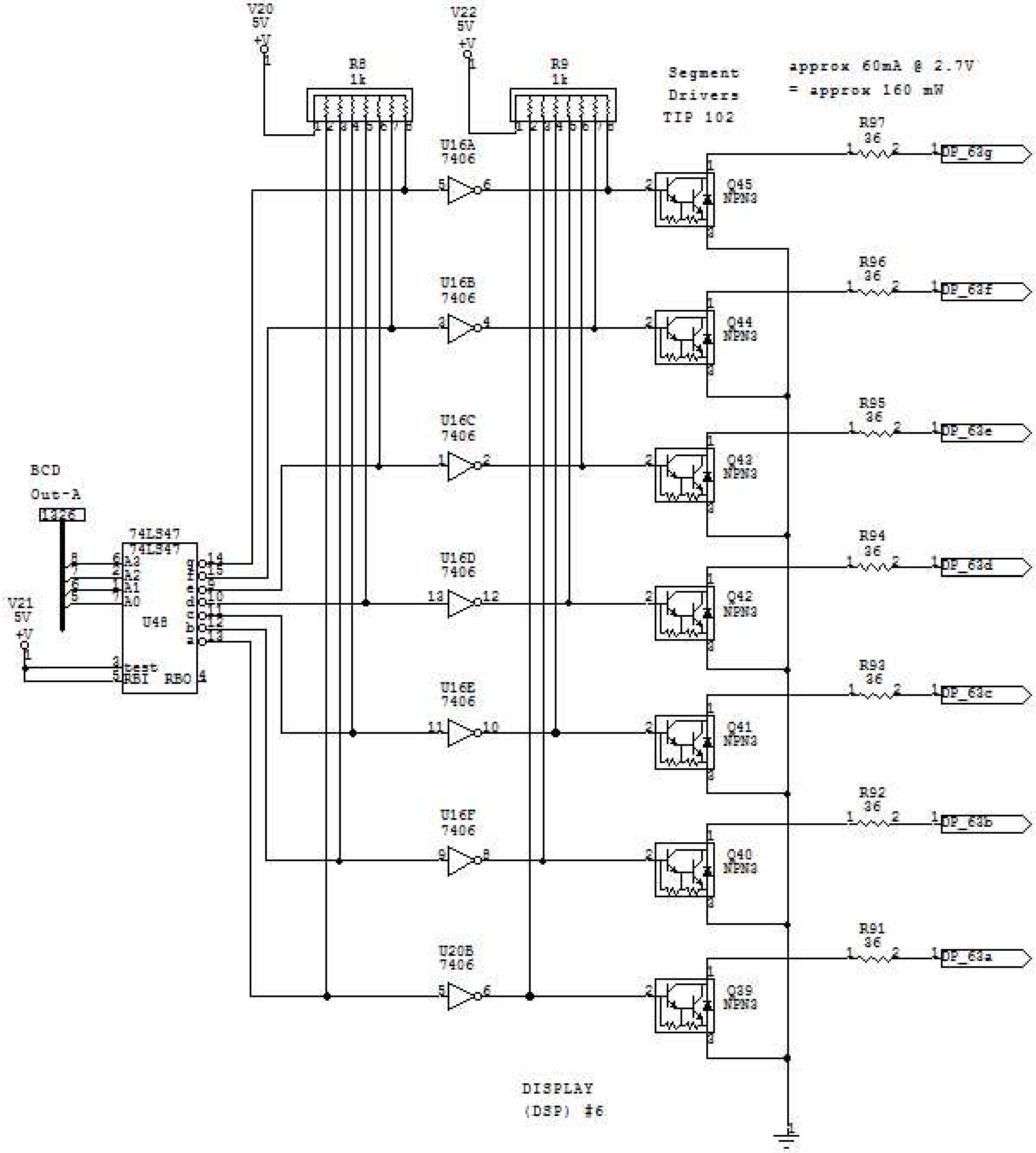
DISPLAY
(DSP) #3

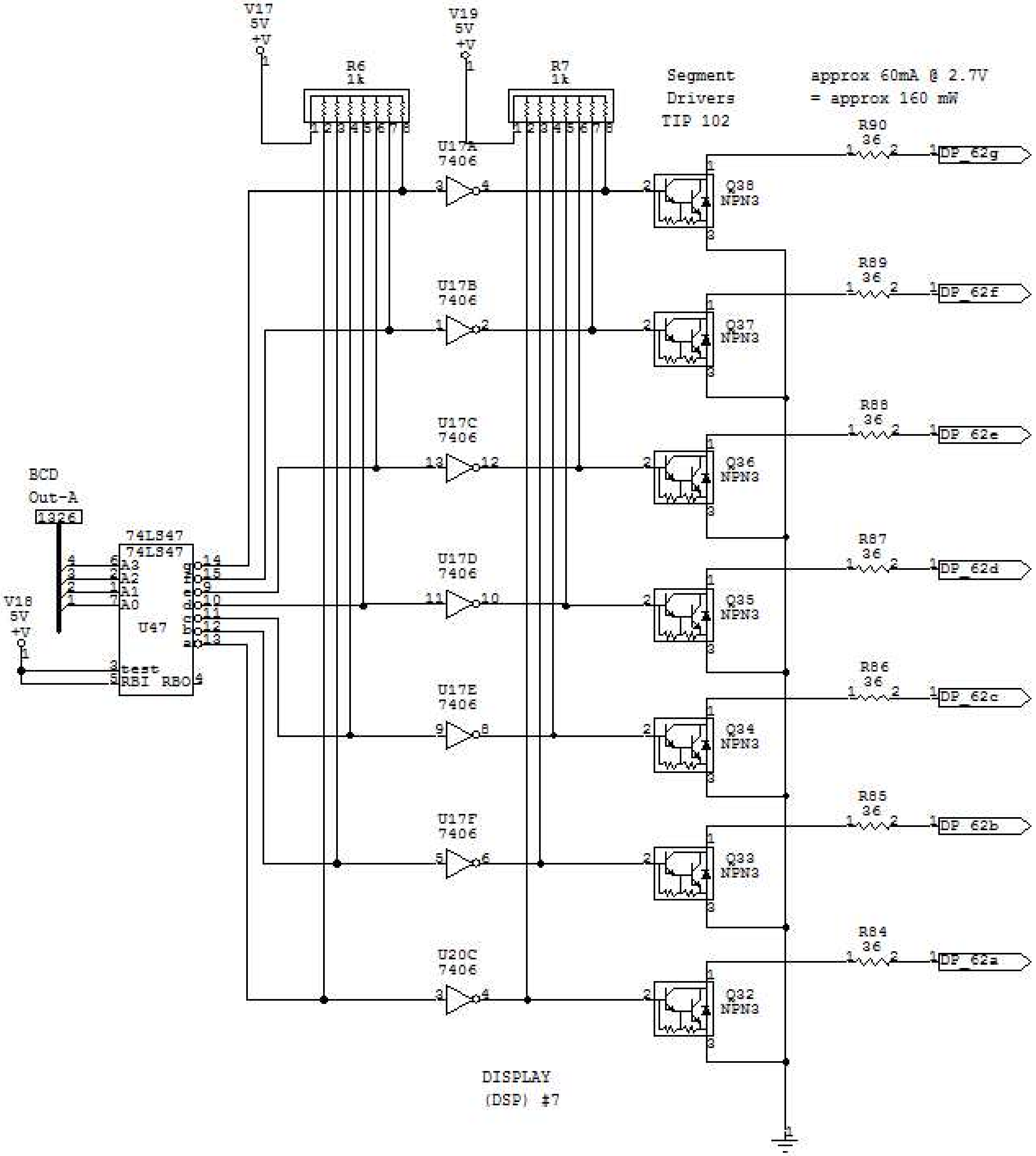


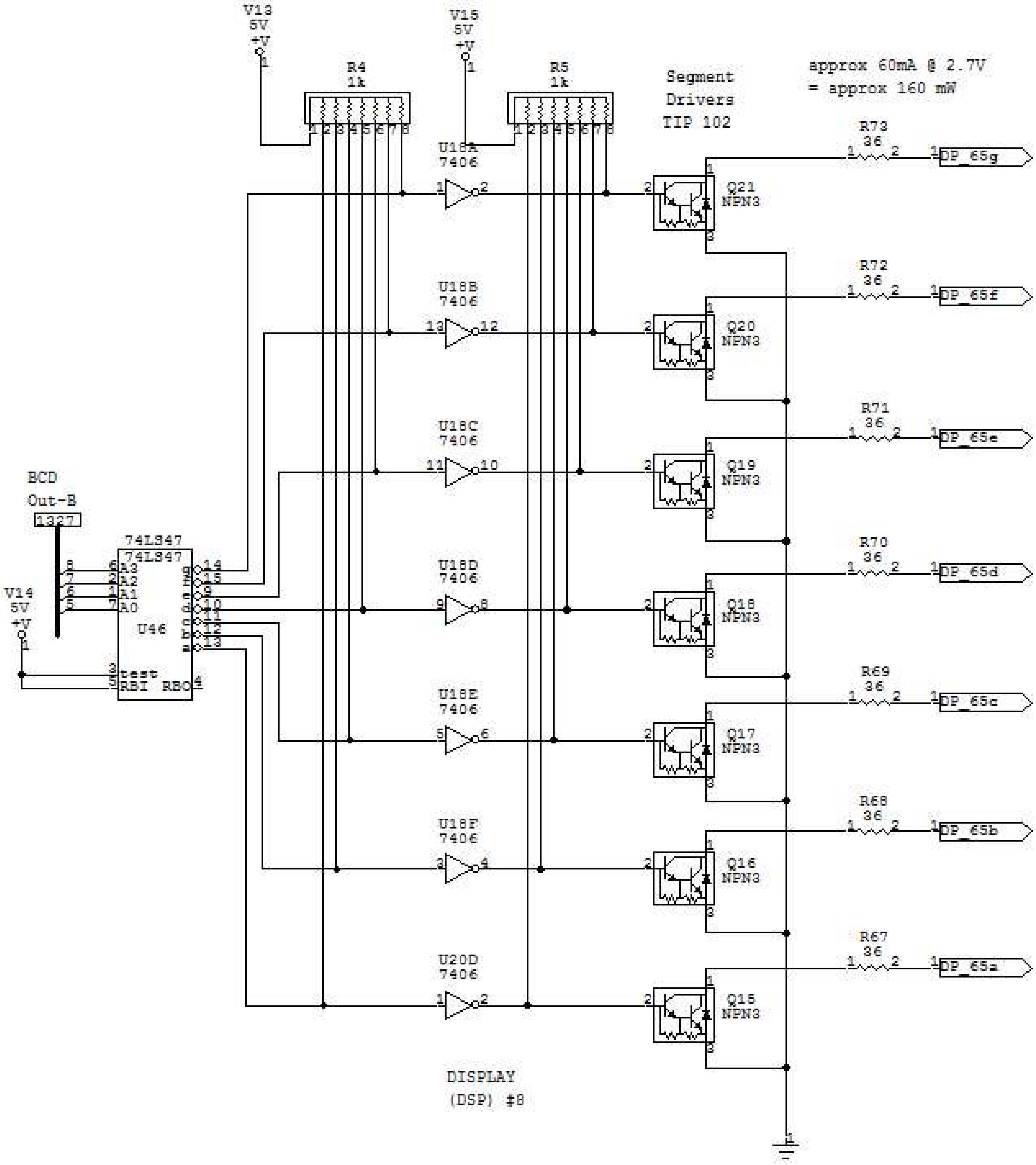
DISPLAY (DSP) #4

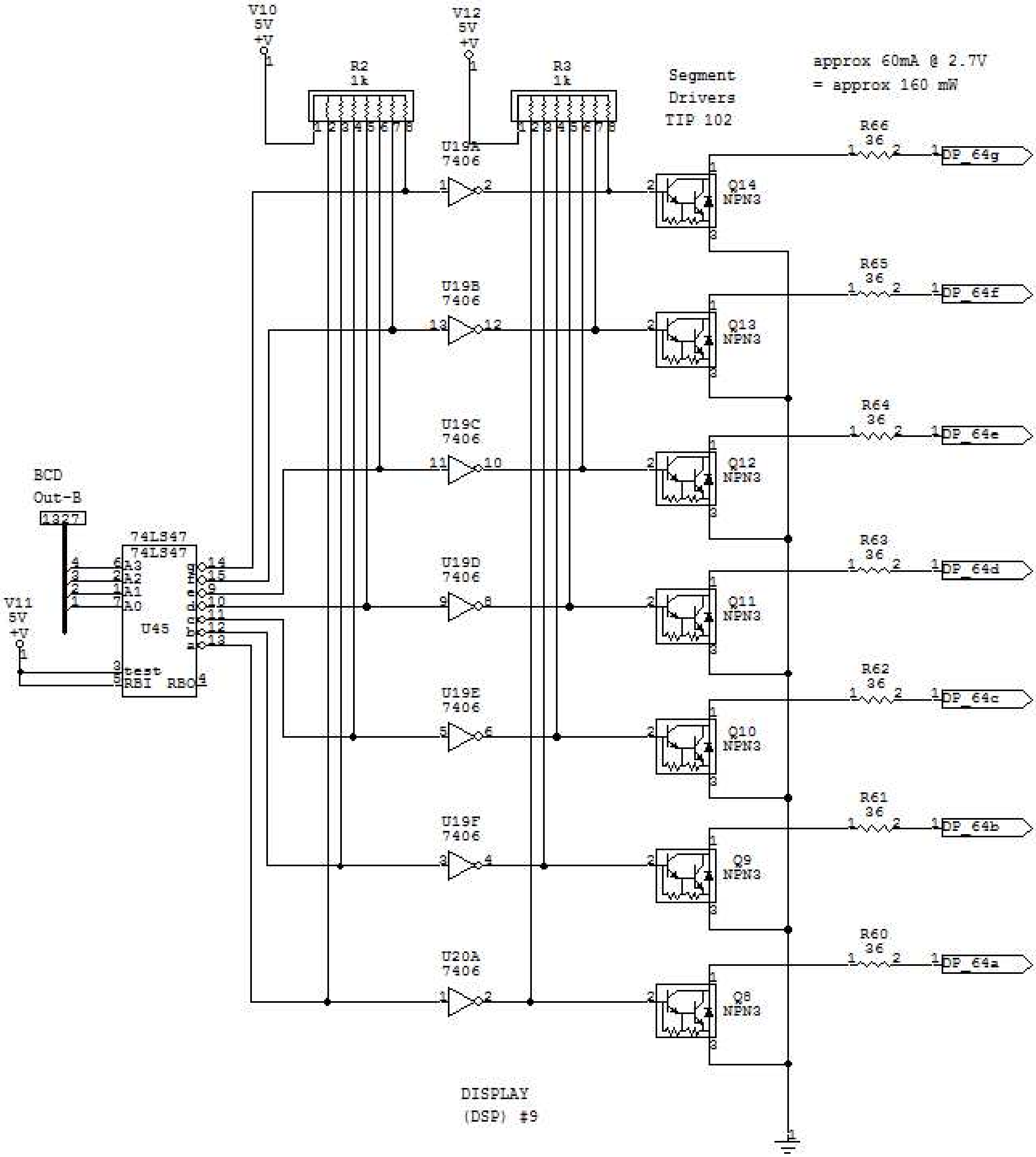


DISPLAY
(DSP) #5


V20
5V
+V
R8
1k
V22
5V
+V
R9
1k
Segment
Drivers
TIP 102
approx 60mA @ 2.7V
= approx 160 mW
U16A
7406
U16B
7406
U16C
7406
U16D
7406
U16E
7406
U16F
7406
U20B
7406
Q45
NPN3
Q44
NPN3
Q43
NPN3
Q42
NPN3
Q41
NPN3
Q40
NPN3
Q39
NPN3
R97
36
R96
36
R95
36
R94
36
R93
36
R92
36
R91
36
DP_6dg
DP_6df
DP_6de
DP_6dd
DP_6dc
DP_6db
DP_6da
BCD
Out-A
1326
74LS47
74LS47
U48
A3
A2
A1
A0
test
RBI
RBO
g
f
e
d
c
b
a
V21
5V
+V
DISPLAY
(DSP) #6

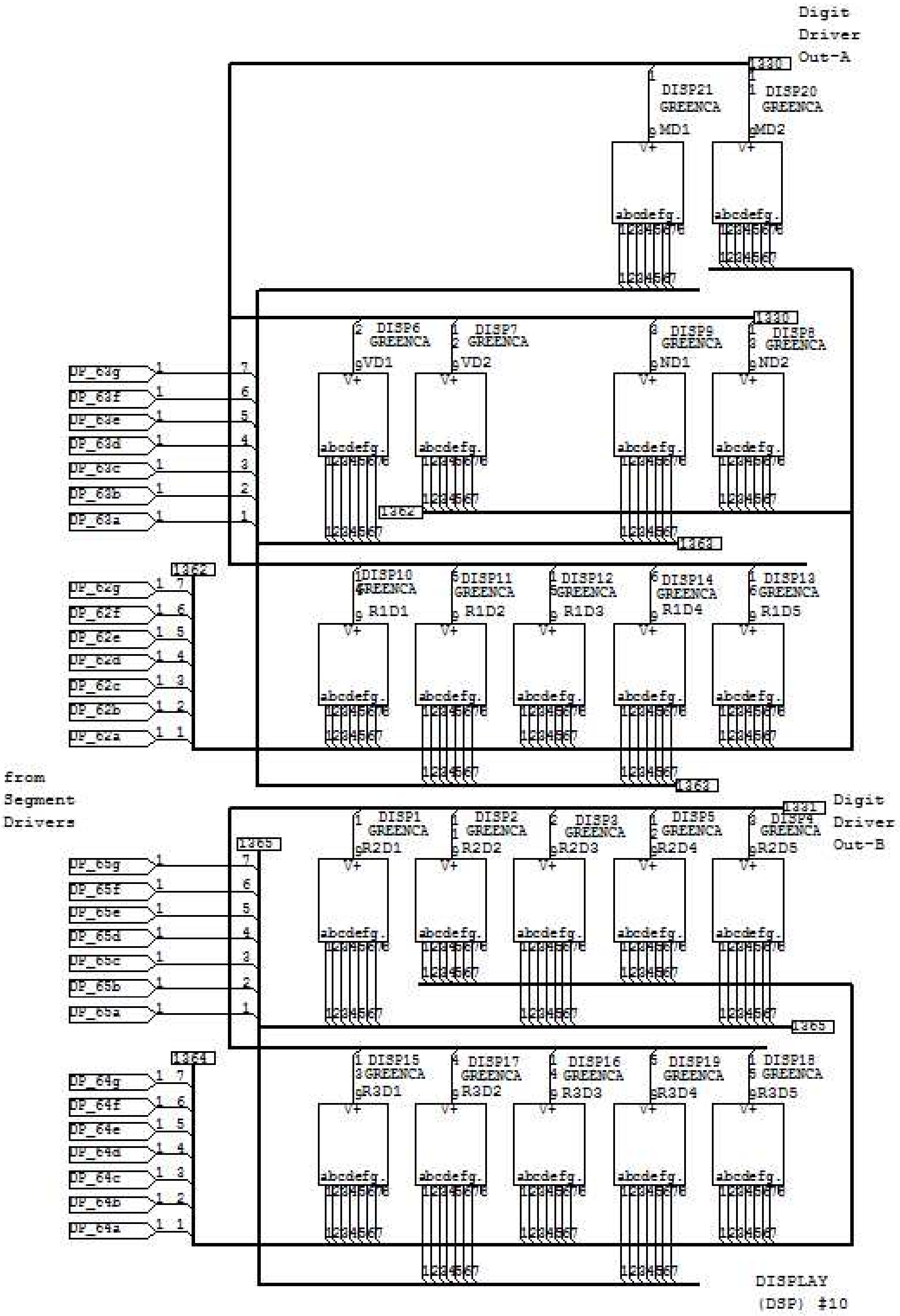

V17
5V
+V
R6
1k
V19
5V
+V
R7
1k
Segment
Drivers
TIP 102
approx 60mA @ 2.7V
= approx 160 mW
R90
36
DP_62g
U17A
7406
Q38
NPN3
U17B
7406
R89
36
DP_62f
Q37
NPN3
U17C
7406
R88
36
DP_62e
Q36
NPN3
BCD
Out-A
1326
74LS47
74LS47
A3
A2
A1
A0
U47
test
RBI
RBO
V18
5V
+V
U17D
7406
R87
36
DP_62d
Q35
NPN3
U17E
7406
R86
36
DP_62c
Q34
NPN3
U17F
7406
R85
36
DP_62b
Q33
NPN3
U20C
7406
R84
36
DP_62a
Q32
NPN3
DISPLAY
(DSP) #7


V13
5V
+V
V15
5V
+V
R4
1k
R5
1k
Segment
Drivers
TIP 102
approx 60mA @ 2.7V
= approx 160 mW
U18A
7406
U18B
7406
U18C
7406
U18D
7406
U18E
7406
U18F
7406
U20D
7406
R73
36
R72
36
R71
36
R70
36
R69
36
R68
36
R67
36
DP_65g
DP_65f
DP_65e
DP_65d
DP_65c
DP_65b
DP_65a
Q21
NPN3
Q20
NPN3
Q19
NPN3
Q18
NPN3
Q17
NPN3
Q16
NPN3
Q15
NPN3
BCD
Out-B
1327
74LS47
74LS47
U46
A3
A2
A1
A0
test
RBI
RBO
V14
5V
+V
DISPLAY
(DSP) #8

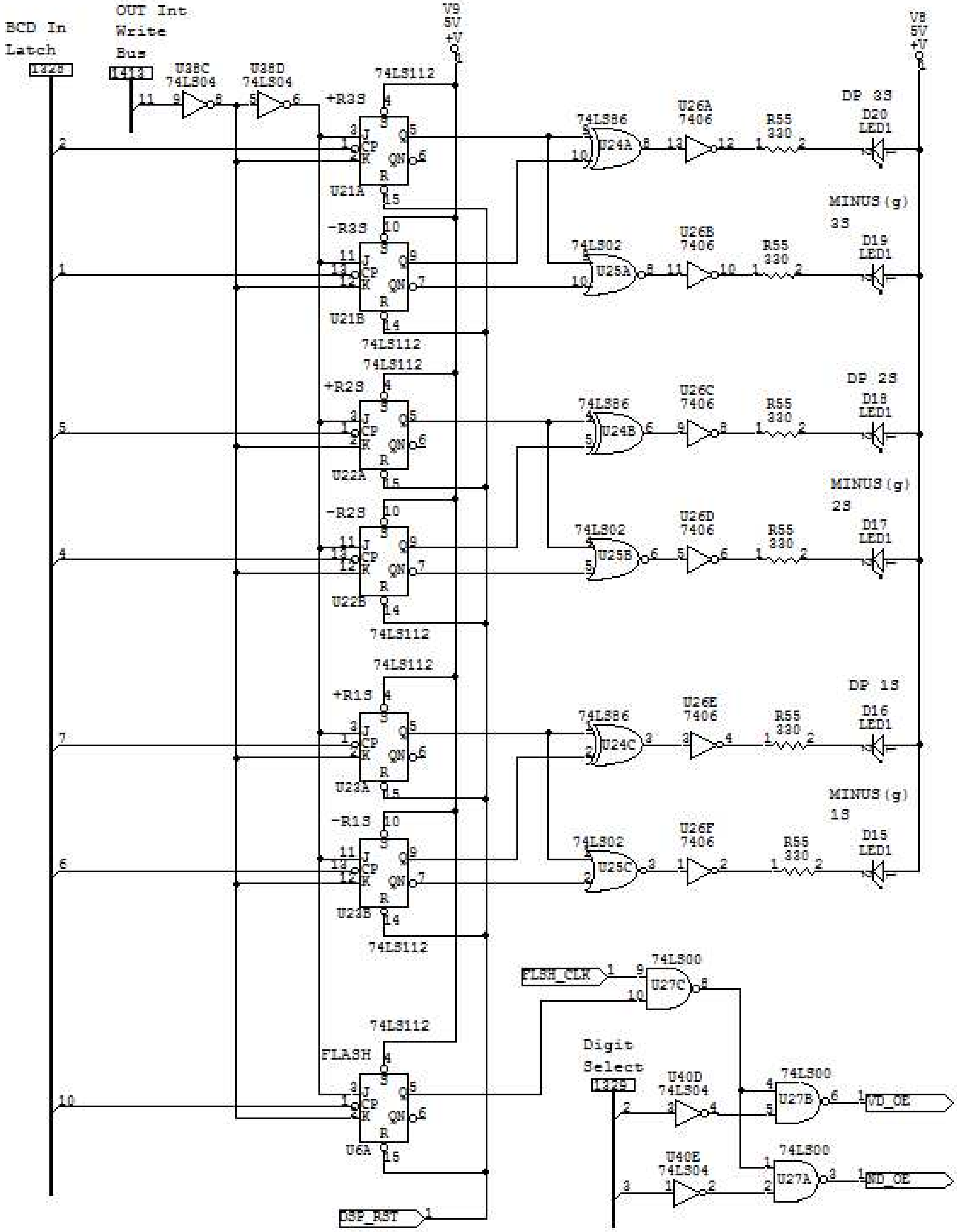


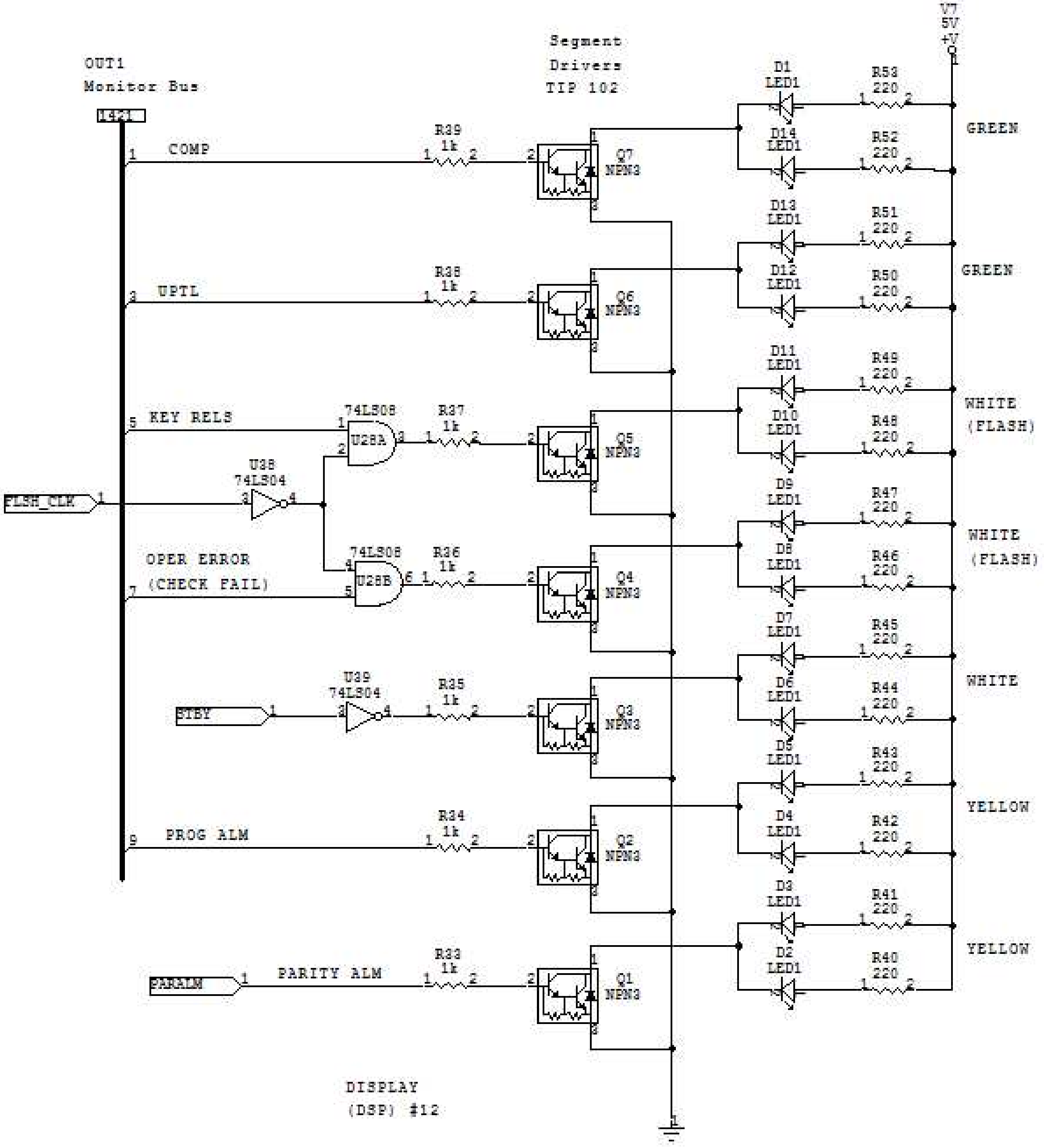
approx 60mA @ 2.7V
= approx 160 mW

DISPLAY
(DSP) #9


Digit
Driver
Out-A
1330
DISP21
GREENCA
MD1
DISP20
GREENCA
MD2
DISP6
GREENCA
VD1
DISP7
GREENCA
VD2
DISP9
GREENCA
ND1
DISP8
GREENCA
ND2
DP_63g
DP_63f
DP_63e
DP_63d
DP_63c
DP_63b
DP_63a
1362
1363
DP_62g
DP_62f
DP_62e
DP_62d
DP_62c
DP_62b
DP_62a
DISP10
GREENCA
R1D1
DISP11
GREENCA
R1D2
DISP12
GREENCA
R1D3
DISP14
GREENCA
R1D4
DISP13
GREENCA
R1D5
from
Segment
Drivers
1331
Digit
Driver
Out-B
1365
DP_65g
DP_65f
DP_65e
DP_65d
DP_65c
DP_65b
DP_65a
DISP1
GREENCA
R2D1
DISP2
GREENCA
R2D2
DISP3
GREENCA
R2D3
DISP5
GREENCA
R2D4
DISP4
GREENCA
R2D5
1364
DP_64g
DP_64f
DP_64e
DP_64d
DP_64c
DP_64b
DP_64a
DISP15
GREENCA
R3D1
DISP17
GREENCA
R3D2
DISP16
GREENCA
R3D3
DISP19
GREENCA
R3D4
DISP18
GREENCA
R3D5
V+
abcdefg.
1234567
DISPLAY
(DSP) #10

DISPLAY
(DSP) #11

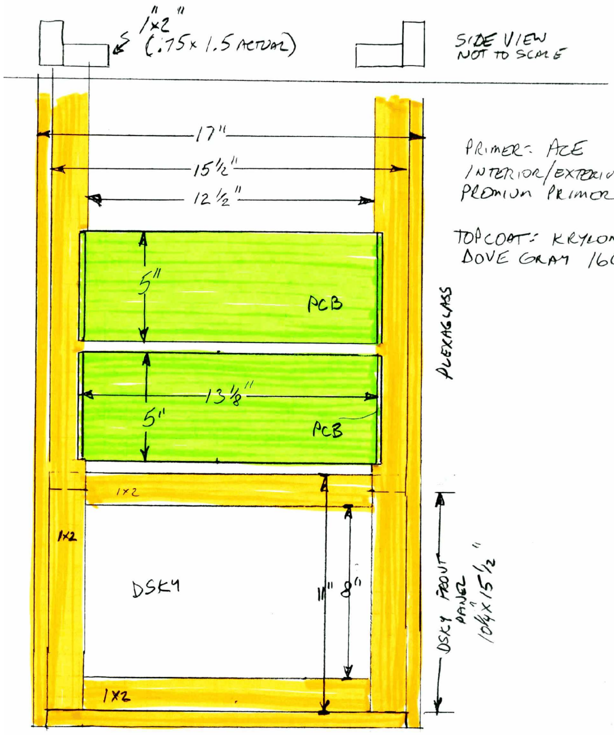



OUT1
Monitor Bus
1421
COMP
UPTL
KEY RELS
FLSH_CLK
OPER ERROR
(CHECK FAIL)
STBY
PROG ALM
PARALM
PARITY ALM
U38
74LS04
74LS08
U28A
74LS08
U28B
U39
74LS04
R39 1k
R38 1k
R37 1k
R36 1k
R35 1k
R34 1k
R33 1k
Segment
Drivers
TIP 102
Q7 NPN3
Q6 NPN3
Q5 NPN3
Q4 NPN3
Q3 NPN3
Q2 NPN3
Q1 NPN3
D1 LED1
D14 LED1
D13 LED1
D12 LED1
D11 LED1
D10 LED1
D9 LED1
D8 LED1
D7 LED1
D6 LED1
D5 LED1
D4 LED1
D3 LED1
D2 LED1
R53 220
R52 220
R51 220
R50 220
R49 220
R48 220
R47 220
R46 220
R45 220
R44 220
R43 220
R42 220
R41 220
R40 220
V7
5V
+V
GREEN
GREEN
WHITE
(FLASH)
WHITE
(FLASH)
WHITE
YELLOW
YELLOW
DISPLAY
(DSP) #12

Fabrication

The IO module is (2) 13"x5" circuit boards, and 1 DSKY panel containing a display driver board, a 7-segment display board, a discrete LED indicator board, and a keyboard.

Module Rack



The module framework is designed to resemble a relay rack, but scaled to fit the circuit board dimensions. It is constructed out of 1"x2" pine and spray-painted semi-gloss gray.

Circuit boards are mounted to the rack by 2 phillips screws at either end. Nylon spacers (1/4") are used as standoffs to hold the board edges above the rack. The boards are mounted so the chips are in the back and the pins are wiring are visible from the front.

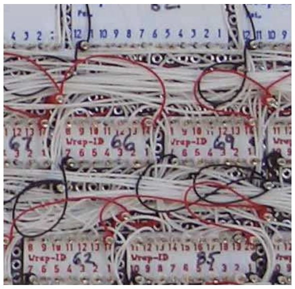
Power is distributed by 2 heavy aluminum bus bars mounted vertically, one per side, on the back of the module. Machine screws are mounted through the bus bars at evenly-spaced intervals to provide connection points for the boards.

Solid copper wire (24 gauge) connects the boards to the bus bars. Ring terminals are used on the bus bar side of the connection. On the circuit board size, the wires are soldered directly to the supply rails.

Materials were purchased from Home Depot, ACE Hardware, and Radio Shack.

Circuit Boards

The circuit boards are 13"x5" general purpose prototyping boards, epoxy glass with double-side plated through pads on 0.1" centers (JAMECO 21477CL).



ICs are mounted in level 3 machine tooled wire-wrap sockets: 8, 14, 16, 20, 24, and 28 pin (JAMECO). Each socket has the pin-out labeled with a wire-wrap socket ID marker, which slips onto the socket before wrapping (JAMECO). The part number is written onto the ID marker.

Sockets are arranged in 4 horizontal rows on each board, with about 10 sockets per row.

Power is distributed on the back-side of each board by bare 24-gauge solid copper wire supply rails soldered at equal intervals to Klipwrap terminals: 3-prong terminals with a square tail for wire-wrapping (JAMECO 34163CL). A +5V rail runs above each row of sockets and a ground rail runs below. Each rail connects directly to the aluminum module power bus using a ring tail connector.

On the pin side of the board, all connections are made with 30 AWG Kynar wire-wrap wire (JAMECO). Red wire is used for direct connections to the +5V supply rail. Black wire is used for direct connections to ground. White wire is used for everything else.

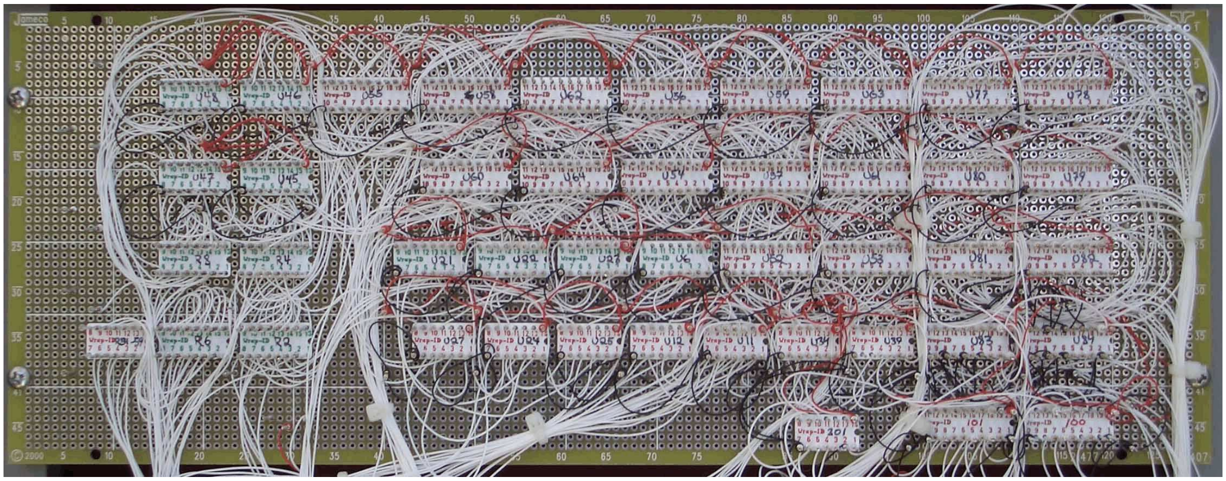
Power connections from the supply rails to each ICs are double-wrapped. Bypassing capacitors (.1 uf disc) are soldered across the supply rails at the Klipwrap terminals; about 1 capacitor for every 2 IC packages.

All connections were stripped and hand-wrapped using a Radio Shack hand-wrap tool. As each connection was made, the corresponding line on the schematic was marked with a colored highlighter.

DIP resistor networks (JAMECO) plugged into 20-pin wire-wrap sockets were used as current limiting resistors for the panel indicators.

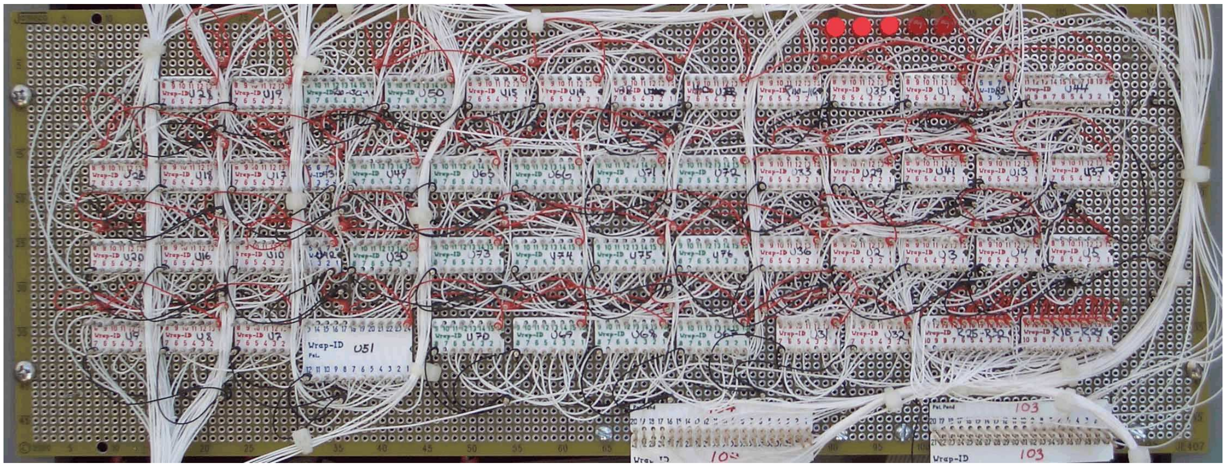
IO Circuit Board A

The A board contains the module interface buffers, input and output registers, and the latches that hold the BCD codes for the 7-segment displays.



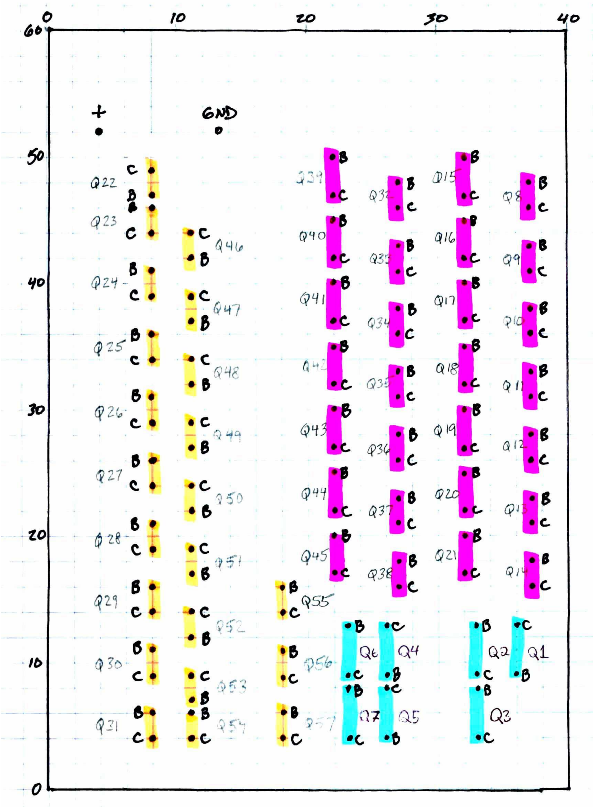
IO Circuit Board B

The B board contains keyboard and display logic. The 40-pin IDE connectors that interface to the other modules are visible at the bottom. The 5 red LEDs show the keyboard code latched into the KBD output register.



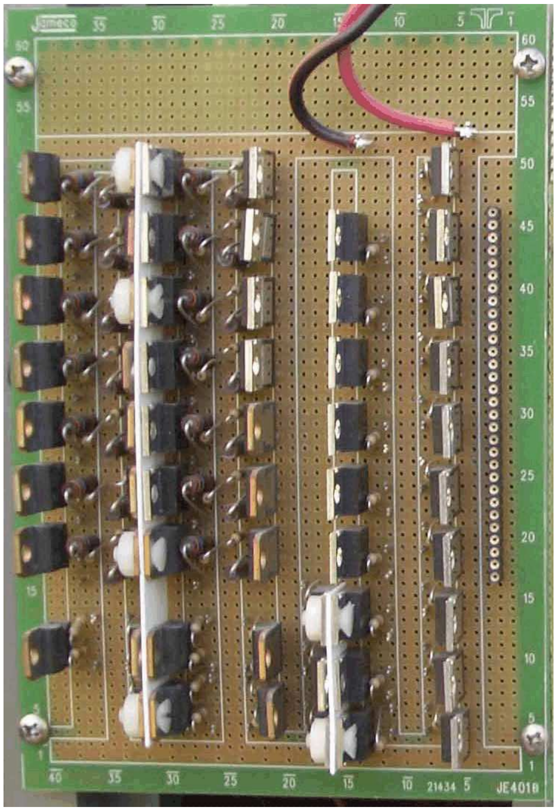
IO Device Driver Board C

The C board contains driver transistors and their associated resistors. The transistors are plastic medium-power complementary silicon: NPN transistors are TIP102, PNP transistors are TIP107. Viewed from the front of the TO-220 case, the base (1) is to the left, collector (2) in the middle, and emitter (3) to the right. The metal tab (4) is the collector.

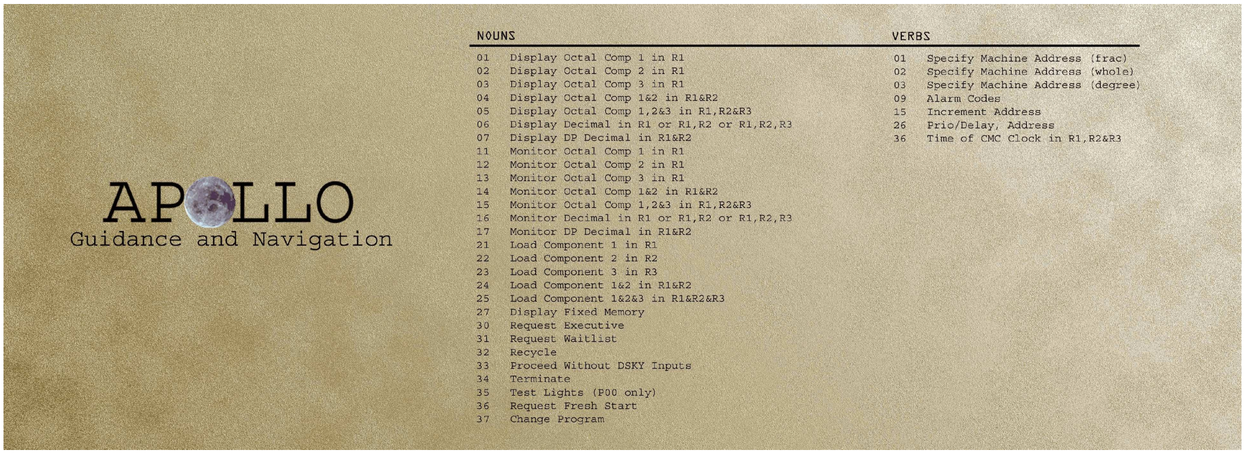


DISPLAY DRIVER PCB

(FOIL SIDE)



An empty space at the top of the IO module rack was filled with a plexiglass panel listing verb and noun codes:



APOLLO

Guidance and Navigation

NOUNS	
01	Display Octal Comp 1 in R1
02	Display Octal Comp 2 in R1
03	Display Octal Comp 3 in R1
04	Display Octal Comp 1&2 in R1&R2
05	Display Octal Comp 1,2&3 in R1,R2&R3
06	Display Decimal in R1 or R1,R2 or R1,R2,R3
07	Display DP Decimal in R1&R2
11	Monitor Octal Comp 1 in R1
12	Monitor Octal Comp 2 in R1
13	Monitor Octal Comp 3 in R1
14	Monitor Octal Comp 1&2 in R1&R2
15	Monitor Octal Comp 1,2&3 in R1,R2&R3
16	Monitor Decimal in R1 or R1,R2 or R1,R2,R3
17	Monitor DP Decimal in R1&R2
21	Load Component 1 in R1
22	Load Component 2 in R2
23	Load Component 3 in R3
24	Load Component 1&2 in R1&R2
25	Load Component 1&2&3 in R1&R2&R3
27	Display Fixed Memory
30	Request Executive
31	Request Waitlist
32	Recycle
33	Proceed Without DSKY Inputs
34	Terminate
35	Test Lights (P00 only)
36	Request Fresh Start
37	Change Program

VERBS	
01	Specify Machine Address (frac)
02	Specify Machine Address (whole)
03	Specify Machine Address (degree)
09	Alarm Codes
15	Increment Address
26	Prio/Delay, Address
36	Time of CMC Clock in R1,R2&R3

Parts (ICs)

IC's, sockets, PCB's, resistors, capacitors, wire-wrap wire were purchased from JAMECO. IDE wire-wrap sockets were from DigiKey. Wire ties, wire-wrap tools, and copper wire were from Radio Shack. IDE ribbon cables were purchased from an online computer supplier.

74LS00	(13)	U27, U27B, U27C, U15C, U15B, U15, U14C, U14B, U14, U29D, U29C, U29B, U34B
74LS02	(3)	U25,U25,U33C
74LS04	(27)	U40E, U40D, U38D, U38C, U40F, U40C, U39E, U39D, U39C, U39B, U41D, U40B, U37F, U39F, U12, U12B, U12C, U12D, U12E, U11F, U11E, U11D, U11C, U11B, U11, U39A, U37
74LS06	(41)	U26F, U26E, U26D, U26C, U26B, U26, U20, U18D, U18C, U18B, U18, U20C, U17E, U17D, U20B, U16F, U16E, U9, U9B, U9C, U9D, U9E, U9F, U10, U10B, U10C, U10D, U7, U7B, U7C, U7D, U7E, U7F, U8, U20, U19F, U19E, U19D, U19C, U19B, U19
74LS08	(1)	U28
74LS10	(1)	U4
74LS20	(5)	U2, U3, U5, U31, U32
74LS27	(2)	U35C, U36
74LS47	(4)	U46, U47, U48, U45
74LS74	(1)	U1
74LS86	(1)	U24C
74LS112	(5)	U6A, U23B, U22B, U21B, U30
74LS138	(9)	U50, U67, U68, U69, U70, U73, U74, U75, U76
74LS148	(4)	U65, U66, U71, U72
74LS154	(1)	U51
74LS161A	(1)	U49
74LS244	(10)	U101, U100, U52, U53, U77, U78, U81, U82, U83, U84
74LS273	(3)	U79, U80, U44
74LS374	(11)	U54, U55, U56, U57, U58, U59, U60, U61, U62, U63, U64
GREENCA	(21)	DISP1, DISP2, DISP3, DISP4,DISP5, DISP6, DISP7, DISP8, DISP9, DISP10, DISP11, DISP12, DISP13, DISP14, DISP15, DISP16, DISP17, DISP18, DISP19, DISP20, DISP21
555	(3)	U85, U42, U43
NPN3	(35)	Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q15, Q16, Q17, Q18, Q19, Q20, Q21, Q32, Q33, Q34, Q35, Q36, Q37, Q38, Q39, Q40, Q41, Q42, Q43, Q44, Q45, Q8, Q9, Q10, Q11, Q12, Q13, Q14
PNP3	(22)	Q22, Q23, Q24, Q25, Q26, Q27, Q28, Q29, Q30, Q31, Q46, Q47, Q48, Q49, Q50, Q51, Q52, Q53, Q54, Q55, Q56, Q57

Power Budget

	qty	mA (ea)	mA (tot)
74LS00	13	2.4	31.2
74LS02	3	2.4	7.2
74LS04	27	3.6	97.2
74LS06	41	3.6	147.6
74LS08	1	4.4	4.4
74LS10	1	1.8	1.8
74LS20	5	1.2	6.0

74LS27	2	3.4	6.8	
74LS47	4	7.0	28.0	
74LS74	1	4.0	4.0	
74LS86	1	6.1	6.1	
74LS112	5	4.0	20.0	
74LS138	9	6.3	56.7	
74LS148	4	12.0	48.0	
74LS154	1	6.2	6.2	
74LS161	1	19.0	19.0	
74LS244	10	32.0	320.0	
74LS273	3	17.0	51.0	
74LS374	11	27.0	297.0	
555 3	3.0	9.0		
GREENCA	21	140.0	2940.0	
LED 25	20.0	500.0		

			4.6	Amps total
			4.1	Amps (excluding single LEDs)